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DESCRIPTION

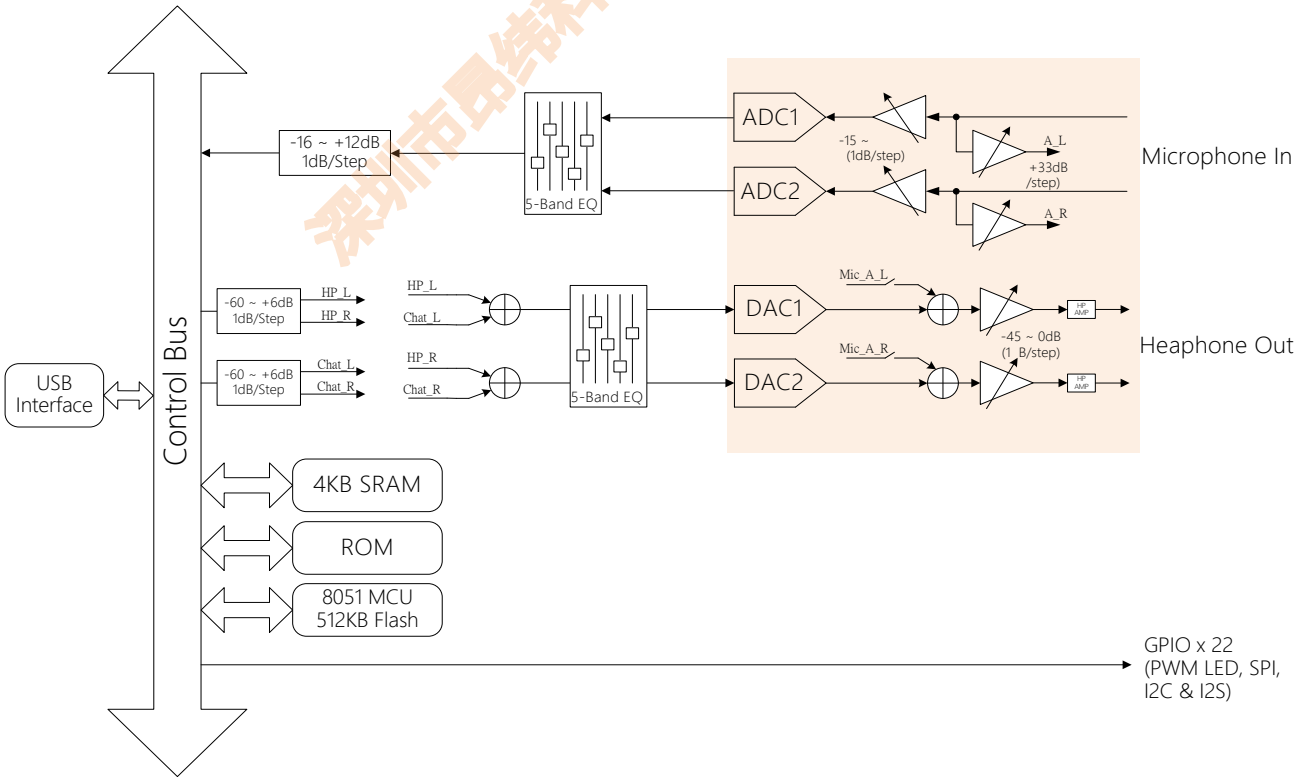
The CM6646X2 is a USB 2.0 high-speed audio codec with 2-channel DAC and 2-channel ADC for Gaming Headset applications. It supports two playback output end-points with independent volume control for game and chat. It also supports mixing function for two playback output end-points. Moreover, the CM6646X2 supports I2C, SPI, UART and GPIOs to communicate with external device. There are 5 bands EQ for both playback and recording interface to compensate the frequency response of speaker or MIC unit or to fulfill personal listening experience.

The CM6646X2 is embedded with 8051 MCU and 512KB flash makes it is very flexible to change the USB topology or communicate with external device by changing internal flash code. It also integrates 6 PWM LED drivers for status indication.

FEATURES

- USB specification 2.0 full-speed/high-speed compliant
- USB audio class 2.0 compliant
- USB human interface device (HID) class 1.1 compliant
- Support USB suspend/resume/reset functions
- Support control, interrupt and isochronous data transfers
- Integrate 2-channel DAC and 2-channel ADC
- True Cap-less/zero-ground headphone driver with patent applied anti-pop technology
- Embedded oscillator for Crystal-less design
- Embedded 7-bits SAR ADC supports Combo jack and Google button detection
- 2 stereo I2S serial audio output/input interfaces
- 1 I2C master, 1 I2C slave, 1 SPI master and 22 GPIOs
- Integrate 6 PWM LED drivers
- Support 5 bands playback and recording EQ
- Support 2 output end-points audio stream mixing function

BLOCK DIAGRAM



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Release notes

Revision	Date	Description
1.00	2025/05/05	- Formal release
1.10	2025/06/30	- Modify Electrical Characteristics

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1. Description and Overview

The CM6646X2 is a USB 2.0 high-speed audio codec with 2-channel DAC and 2-channel ADC for Gaming Headset applications. It supports two playback output end-points with independent volume control for game and chat. It also supports mixing function for two playback output end-points. Moreover, the CM6646X2 supports I2C, SPI, UART and GPIOs to communicate with external device. There are 5 bands EQ for both playback and recording interface to compensate the frequency response of speaker or MIC unit or to fulfill personal listening experience.

The CM6646X2 is embedded with 8051 MCU and 512KB flash makes it is very flexible to change the USB topology or communicate with external device by changing internal flash code. It also integrates 6 PWM LED drivers for status indication.

2. Ordering Information

Product	Package Marking	Package Type	Transport Media
CM6646X2	CM6646X2	QFN-68(7x7mm)	Tray

3. Features

3.1 USB Compliance

- USB 2.0 full-speed/high speed compliant
- USB audio class 2.0 compliant
- USB human interface device (HID) class 1.1 compliant
- Support USB suspend/resume/reset functions
- Support control, interrupt and isochronous data transfers

3.2 Integrated 8051 Micro Processor

- Embedded 8051 micro-processor handles the USB transfers(control, isochronous and interrupt)
- Communicate with external peripheral devices(I2C, SPI, GPIO, etc.)
- The MCU speed is programmable from 3.072 to 65.536 MHz
- HID interrupts can be implemented via firmware codes
- Provide HW configuration flexibility with a firmware code upgrade
- VID/PID/product string and others can be customized via firmware code programming

3.3 Control Interface

- 1 Master I2C control interface to communicate with external devices or EEPROM, the master I2C speed supports standard mode(100KHz) and fast mode(400KHz)
- 1 Slave I2C control interface for external MCU communication, the slave I2C speed supports standard mode(100KHz) and fast mode(400KHz)
- 1 SPI master(share with GPIO), supports speed up to 24.576 Mb/s (Depends on MCU speed)
- 22 GPIOs(programmable multi functions I/O)
- 6 PWM LED drivers output share with GPIO
-

3.4 Audio Engine and Codec

- Playback Stream:
  - Stereo DAC:

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- Sample Rates: 44.1/48/88.2/96/176.4/192KHz
- Bit Depth: 16/24/32 bits
- Analog Gain Range: -45 ~ 0dB, 1dB/step
- Digital Gain Range: -60 ~ +6dB, 1dB/step
- True Cap-less/zero-ground headphone driver with patent applied anti-pop technology

➢ Stereo I2S output interface:

- Sample Rates: 44.1/48/88.2/96/176.4/192KHz
- Bit Depth: 16/24/32 bits

➢ 5-band Digital Parametric Equalizer

Notes: To support 2 output end-points audio stream mix together, the audio format of the 2 audio output end-points must be the same.

- Recording Stream:

➢ Stereo ADC

- Sample Rates: 44.1/48/88.2/96/176.4/192KHz
- Bit Depth: 16/24/32 bits
- Microphone gain range: -15~ +33dB, 1dB/step
- Digital Gain Range: -16 ~ +12dB, 1dB/step

➢ Stereo I2S input interface:

- Sample Rates: 44.1/48/88.2/96/176.4/192KHz
- Bit Depth: 16/24/32 bits

➢ 5-band Digital Parametric Equalizer

- A-A Mixer (Sidetone):

➢ Analog input to analog output mixer path with independent volume control: -15 ~ +33dB, 1dB/step

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3.5 General

- Embedded USB 2.0 transceiver and power-on reset circuit
- Bus-power and self-power options
- Embedded oscillator for Crystal-less design
- True Cap-less/zero-ground headphone driver with patent applied anti-pop technology
- Single power supply with embedded 5V to 3.3V regulator
- 3.3V digital I/O pads with 5V tolerance
- Compliant with USB IF certification requirements
- QFN-68 package (7 x 7 mm)

3.6 Xear™ Sound Processing

- Xear 3D Sound Anchor(w/ headtracking)

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- Xear™ Surround Headphone
- Xear™ Software 10 Band Equalizer
- Xear™ Audio Brilliant
- Xear™ Dynamic Bass
- Xear™ Voice Clarity
- Xear™ Smart Volume
- Xear™ Magic Voice
- Xear™ AI Noise Cancellation

4. Applications

- PC Gaming Headset with 2-Output End Point mixing function
- USB Audio Dongle
- Live streaming mixer box

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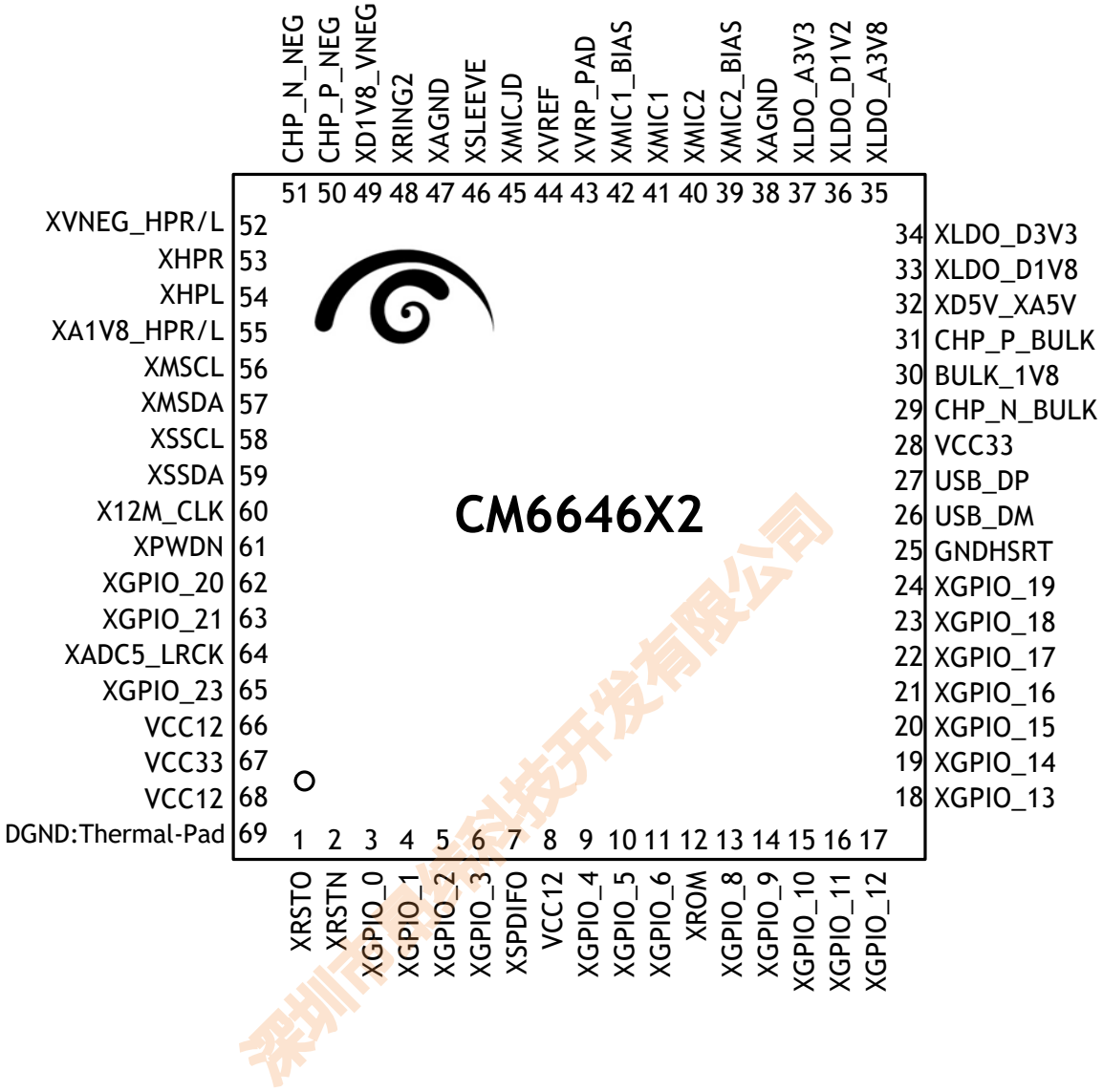
5. Pin Assignment

5.1 Pin-out Diagram



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5.2 I/O Type Description

I/O Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIL	Digital Input with internal pull-down 50K
DIH	Digital Input with internal pull-up 50K
DIOL	Digital Input/Output with internal pull-down 50K
DIOH	Digital Input/Output with internal pull-up 50K
IOU	USB related IO
PWRO	Power output pin
PWRI	Power input pin
GND	Ground related pin

5.3 Pin Description

Pin #	Symbol	I/O	Description
USB 2.0 BUS Interface			
27	USB_DP	IOU	USB 2.0 data positive
26	USB_DM	IOU	USB 2.0 data negative
Power/Ground			
25	GNDHSRT	GND	Digital ground
32	XD5V_XA5V	PWRI	Digital/Analog supply power; Connect to capacitor filter
38	XAGND	GND	Analog ground
47	XAGND	GND	Analog ground
30	BULK_1V8	PWRO	DC to DC 1.8V output, 40mA driving current ; Connect to capacitor filter
49	XD1V8_VNEG	PWRI	DC to DC 1.8V input Input power of negative charge pump ; Connect to capacitor filter
55	XA1V8_HPR/L	PWRI	Analog 1.8V input Positive Power of headphone driver R/L CH ; Connect to capacitor filter
52	XVNEG_HPR/L	PWRO	DC to DC -1.8V output, 10mA driving current ; Connect to capacitor filter
35	XLDO_A3V8	PWRO	LDO 3.8V output, 20mA driving current ; Connect to capacitor filter
37	XLDO_A3V3	PWRO	LDO 3.3V output, 20mA driving current ; Connect to capacitor filter
34	XLDO_D3V3	PWRO	LDO 3.3V output, 30mA driving current ; Connect to capacitor filter
33	XLDO_D1V8	PWRO	LDO 1.8V output, 20mA driving current ; Connect to capacitor filter
36	XLDO_D1V2	PWRO	LDO 1.2V output, 10mA driving current ; Connect to capacitor filter
28	VCC33	PWRI	VCC 3.3V input Digital supply voltage 3.3V for digital I/O
8	VCC12	PWRI	VCC 1.2V input Digital supply voltage 3.3V for digital core
66	VCC12	PWRI	VCC 1.2V input Digital supply voltage 3.3V for digital core

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67	VCC12	PWRI	VCC 1.2V input Digital supply voltage 3.3V for digital core
68	VCC12	PWRI	VCC 1.2V input Digital supply voltage 3.3V for digital core
69		GND	DGND=Thermal pad
Analog			
44	XVREF	AO	Voltage reference for common mode voltage (~1.5V)
43	XVRP_PAD	AO	Voltage reference for DAC (~3.1V)
42	XMIC1_BIAS	AO	Microphone 1 bias volage output (~3.1V)
41	XMIC1	AI	Microphone 1 input
39	XMIC2_BIAS	AO	Microphone 2 bias volage output (~3.1V)
40	XMIC2	AI	Microphone 2 input
45	XMICJD	AO	Combo jack detect and auto switch, detect combo jack type and switch to XRING2 or XSLEEVE
46	XSLEEVE	AI	Combo jack connectoe: Sleeve
48	XRING2	AI	Combo jack connector: Ring2
31	CHP_P_BULK	AO	Charge pump positive output of DC to DC
29	CHP_N_BULK	AO	Charge pump negative output of DC to DC
50	CHP_P_NEG	AO	Charge pump positive output of high negative DC to DC
51	CHP_N_NEG	AO	Charge pump negative output of high negative DC to DC
54	XHPL	AO	Headphone driver output L CH
53	XHPR	AO	Headphone driver output R CH
S/PDIF I/O			
7	XSPDIFO	DO	S/PDIF transmitter
GPIO			
3	XGPIO_0	DIOL	1). General purpose input/output 0 (default input) 2). LED module 1 output 3). R8051 SPI master clock output, Internal pull low, 4mA driving current
4	XGPIO_1	DIOL	1). General purpose input/output 1 (default input) 2). LED module 2 output 3). R8051 SPI master data output, Internal pull low, 4mA driving current
5	XGPIO_2	DIOL	1). General purpose input/output 2 (default input) 2). LED module 3 output 3). R8051 SPI master data input, Internal pull low, 4mA driving current
6	XGPIO_3	DIOL	1). General purpose input/output 3 (default input) 2). LED module 4 output 3). R8051 SPI master chip enable 0 output, Internal pull low, 4mA driving current
9	XGPIO_4	DIOL	1). General purpose input/output 4 (default input) 2). LED module 5 output 3). I2C slave interrupt output to external MCU Internal pull low, 4mA driving current
10	XGPIO_5	DIOL	1). General purpose input/output 5 (default input) 2). LED module 6 output 3). I2C slave data ready indication output Internal pull low, 4mA driving current
11	XGPIO_6	DIOL	General purpose input/output 6 (default input) Internal pull low, 4mA driving current
13	XGPIO_8	DIOL	1). General purpose input/output 8 (default input) 2). I2S DAC4 master clock output Internal pull low, 4mA driving current
14	XGPIO_9	DIOL	1). General purpose input/output 9 (default input) 2). I2S DAC4 bit clock input/output Internal pull low, 4mA driving current

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15	XGPIO_10	DIOL	1). General purpose input/output 10 (default input) 2). I2S DAC4 left/right clock input/output Internal pull low, 4mA driving current
16	XGPIO_11	DIOL	1). General purpose input/output 11 (default input) 2). I2S DAC4 serial data output Internal pull low, 4mA driving current
17	XGPIO_12	DIOL	1). General purpose input/output 12 (default input) 2). LED module 1 output 3). I2S DAC5 master clock output Internal pull low, 4mA driving current
18	XGPIO_13	DIOL	1). General purpose input/output 13 (default input) 2). LED module 2 output 3). I2S DAC5 bit clock input/output Internal pull low, 4mA driving current
19	XGPIO_14	DIOL	1). General purpose input/output 14 (default input) 2). LED module 3 output 3). I2S DAC5 left/right clock input/output Internal pull low, 4mA driving current
20	XGPIO_15	DIOL	1). General purpose input/output 15 (default input) 2). I2S DAC5 serial data output Internal pull low, 4mA driving current
21	XGPIO_16	DIOL	1). General purpose input/output 16 (default input) 2). I2S ADC4 master clock output Internal pull low, 4mA driving current
22	XGPIO_17	DIOL	1). General purpose input/output 17 (default input) 2). I2S ADC4 bit clock input/output Internal pull low, 4mA driving current
23	XGPIO_18	DIOL	1). General purpose input/output 18 (default input) 2). R8051 serial 1 interface transmit data, TXD1 3). I2S ADC4 left/right clock input/output Internal pull low, 4mA driving current
24	XGPIO_19	DIOL	1). General purpose input/output 19 (default input) 2). R8051 serial 1 interface transmit data, RXD1 3). I2S ADC4 serial data input Internal pull low, 4mA driving current
62	XGPIO_20	DIOL	1). General purpose input/output 20 (default input) 2). LED module 4 output 3). R8051 I2C serial clock 4). I2S ADC5 master clock output Internal pull low, 4mA driving current
63	XGPIO_21	DIOL	1). General purpose input/output 21 (default input) 2). LED module 5 output 3). R8051 I2C serial data 4). I2S ADC5 bit clock input/output Internal pull low, 4mA driving current
64	XADC5_LRCK	DIOL	1). I2S ADC5 left/right clock input/output
65	XGPIO_23	DIOL	1). General purpose input/output 23 (default input) 2). R8051 Timer 2 capture trigger input 4). I2S ADC5 serial data input Internal pull low, 4mA driving current
I2C Master Serial Bus			
56	XMSCL	DIOH	1). I2C master serial clock 2). R8051 I2C serial clock
57	XMSDA	DIOH	1). I2C master serial data 2). R8051 I2C serial data
I2C Slave Serial Bus			

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58	XSSCL	DIOH	1). I2C slave serial clock 2). R8051 I2C serial clock (This function is disabled, if R8051 I2C is connected to XMSCL and XMSDA)
59	XSSDA	DIOH	1). I2C slave serial data 2). R8051 I2C serial data (This function is disabled, if R8051 I2C is connected to XMSCL and XMSDA)
Miscellaneous			
1	XRSTO	DIOL	External codec reset output (default tri-state)
2	XRSTN	DIH	Reset input, active low
12	XROM	DIL	Reserve for restore to ROM mode
60	X12M_CLK	DIOL	12 MHz clock output
61	XPWDN	DIOL	Power down output signal for external device output (default tri-state)

6. Function Description

6.1 USB Topology

The CM6646X2 USB Topology is programmable by changing firmware. If the internal firmware is empty, the CM6646X2 will report a WinUSB device to the system. It is used to load the firmware.

6.2 USB Endpoint

All USB devices must support a control pipe at endpoint number zero (default control pipe). The endpoint table of CM6646X2 is listed as follows.

EndpointNumber	Direction	Type	Description
0	IN	Control	
	OUT		
1	IN	Isochronous	Audio, Recording
3	IN	Feedback	Audio, Playback
	OUT	Isochronous	
4	IN/OUT	Interrupt A	
C	IN	Feedback	Audio, playback
	OUT	Isochronous	
E	IN	Isochronous	Audio, Recording
F	IN/OUT	Interrupt B	

6.3 S/PDIF Interface

SPDIF is an audio transmission format in digital domain. The data stream format is illustrated in Fig. 6.3.1. The maximum unit of the S/PDIF stream is a block. A block is composed of 192 frames, and each frame is composed of two subframes. One frame contains one audio sample, so the frame rate is equal to the sampling rate. The left channel audio data is carried by bit slot 4-27 (or time slot 4-27) of subframe A, and right channel is carried by bit slot 4-27 of subframe B. The Sync slot takes preamble signal which is used to label the beginning of a subframe. There are three types for preamble signal, the first is B type, used only in the first subframe of a block; the W type, used in all subframe B; the M format, used in all subframe A, besides the first subframe of a block. The block format is shown in Fig. 7.3.1. The logical level at the start of a bit is always inverted to the level at the end of the previous bit. The level at the end of a bit is equal (a 0 transmitted) or inverted (a 1 transmitted) to the start of that bit.

The S/PDIF data signal is coded by the “biphase-mark-code,” which is a kind of phase modulation. It is illustrated in Fig. 6.3.2. The base clock of a S/PDIF signal is twice the bit rate, and the frequency of the base clock is only determined by the sampling rate. The period of the base clock is called the Unit interval (UI). For example, for a 48KHz 2-channel S/PDIF signal, the frame rate is also 48KHz, so a frame period is 20.833us, and a subframe period is 10.416us. A subframe contains 32-bit slot, so a bit slot period is 325.52ns. As we said above, the base clock is twice the bit rate. Therefore, the period of the base clock is 162.76ns. In other words, the frequency of base clock is 6.144 MHz. Bi-phase coding can prevent PCM data from DC isolated and insensitive to level polarity. A maximum up to 24

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data bits can be transmitted by the S/PDIF signal, and the sequence is from LSB to MSB.

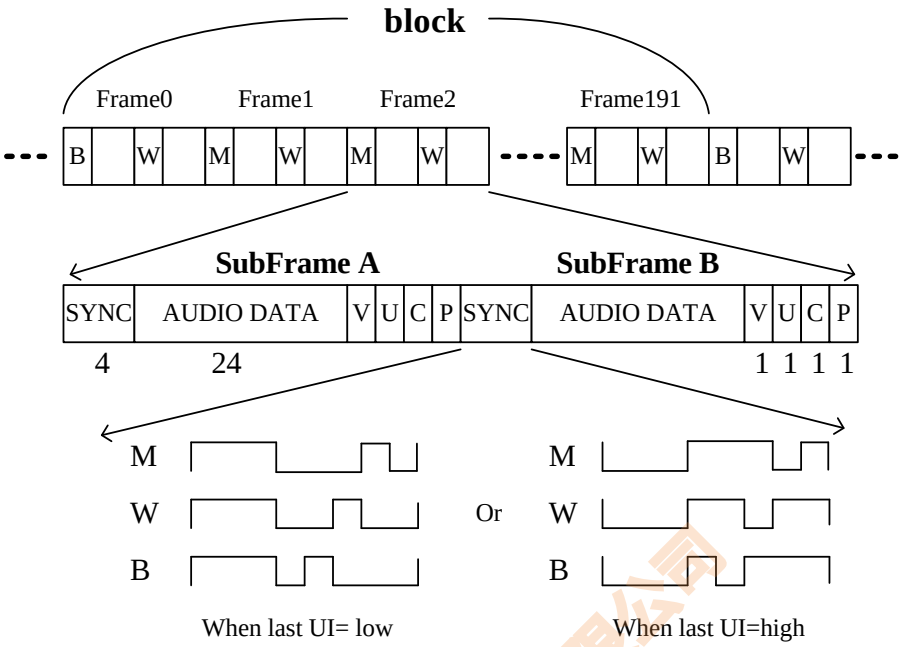

Fig. 6.3.1 S/PDIF Frame format.

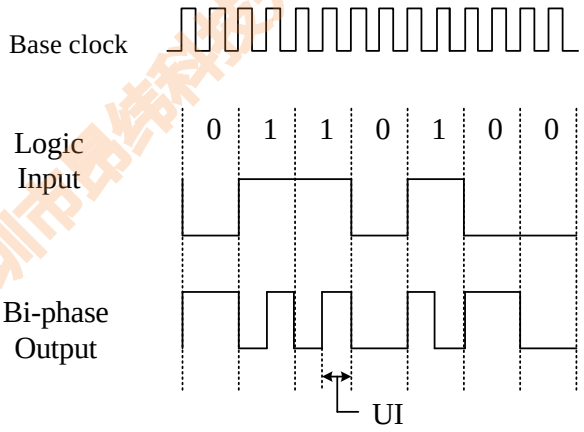

Fig. 6.3.2 S/PDIF biphase-mark-code (BMC).

6.4 Two-Wire Master and Slave Serial Buses (I2C)

The 2-wire master and slave serial buses are designed separately in the CM6646X2.

6.4.1 The Concept of Two-Wire Bus

The 2-wire bus, as its name reveals, has 2 lines. One is the serial clock line (*SCL*), and the other is the serial data line (*SDA*). Both of them are operated under open drain. That means if the 2 lines are not driven by a master or a slave, they are pulled high by the external pull-up resistors as indicated by Fig. 6.4.1.1. A device connected on the bus can be recognized as a master or a slave when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is

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considered a slave. Another concept that we should know is the transmitter-receiver relation. The transmitter is the device which sends data to the bus, and receiver is the device which receives data from the bus. Note that the definition of transmitter-receiver is different from that of master-slave. We will use these terms to explain 2-wire read/write transactions later. The CM6646X2 use 7 bits to address the slave devices such as codecs, so theoretically, the 2-wire bus is able to connect 128 slave devices. However, in the audio system application, the limitation is on the codecs, not on the CM6646X2. Usually, the codecs which support 2-wire bus only have one or two pins to select their address. Therefore, two or four codecs is allowed in the system indicated by Fig. 6.4.1.1, unless the codecs are from different manufactures. In the MCU application, the CM6646X2 is a slave device, and it can be addressed by the MCU via four different addresses, 0001000b, 0001001b, 0001010b, 0001011b.

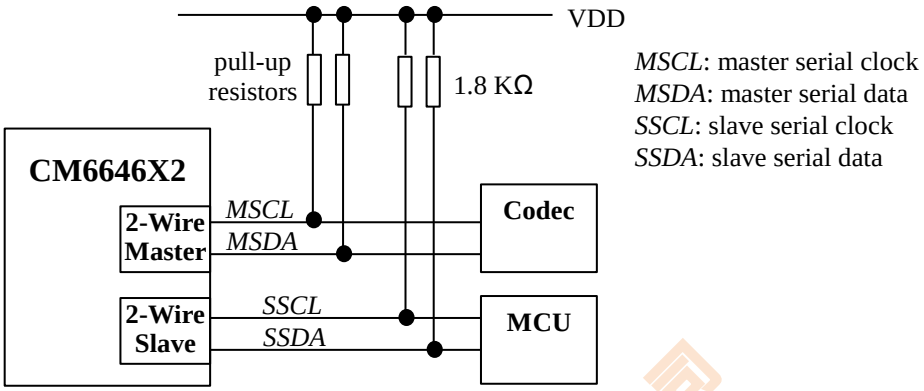

Fig. 6.4.1.1 The connection of 2-wire master and slave buses.

6.4.2 Start and Stop Condition

For a 2-wire bus transaction, the start and stop condition is defined as follows and shown in Fig.6.4.2.1.

- Start: a high to low transition on the *SDA* line while *SCL* is high.
- Stop: a low to high transition on the *SDA* line while *SCL* is high.

Start and stop conditions always generated by the master device. The bus is considered to be busy after the start condition. The bus is considered to be free again after the stop condition.

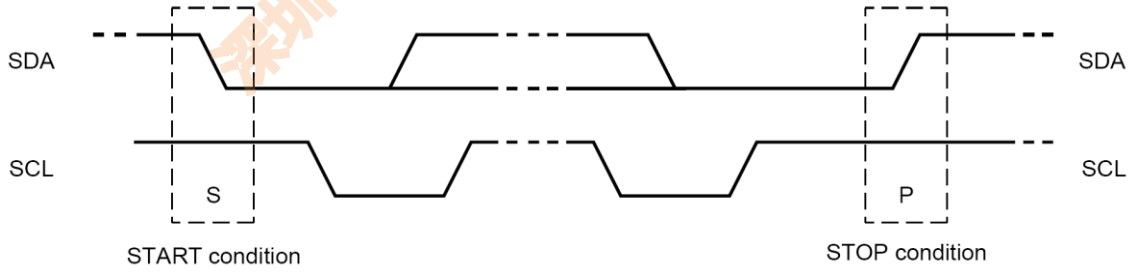

Fig. 6.4.2.1 Start and stop conditions of 2-wire bus.

6.4.3 Bit Transfer

The data on the *SDA* line must be stable during the high period of the clock. The state of the data line can only transit when the clock signal on *SCL* line is low. The bit transfer is indicated in Fig. 6.4.3.1.

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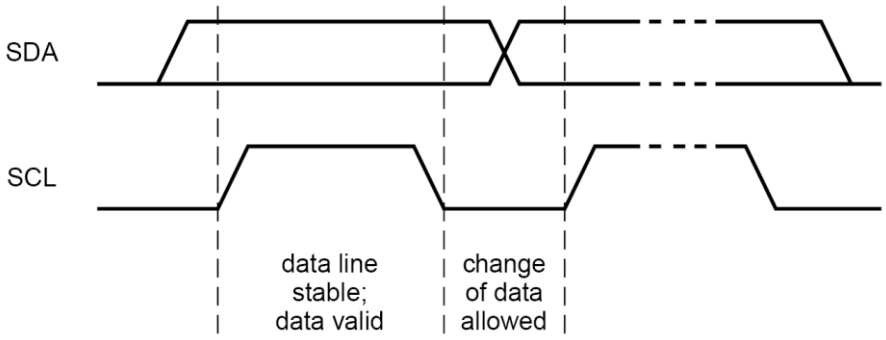

Fig. 6.4.3.1 Bit transfer of 2-wire bus.

6.4.4 Transferring Data with Read/Write Transactions and Acknowledge

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is 3 or 4 bytes in the CM6646X2. The first byte is always the address byte which is composed of the 7-bit address and 1 read/write bit, listed in Fig. 6.4.4.1 For a write transaction, the second byte is called Memory Address Pointer (MAP), which is usually used to indicate the target register in the slave device that the followed third and fourth bytes will be applied on. For a read transaction (only 3 bytes), the second and third bytes is the data returned by the slave device. Each byte has to be ended by an acknowledge bit. Data is transferred with the most significant bit first.

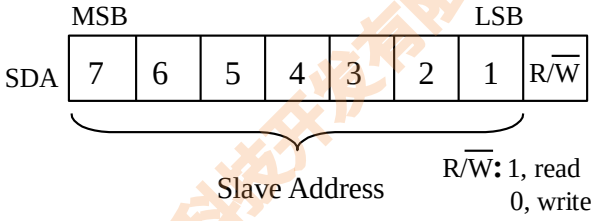

Fig. 6.4.4.1 The first byte after start condition.

The 2-wire master bus of the CM6646X2 supports read/write transactions. All these transactions are depicted in Fig. 6.4.4.2 to give a whole picture about what the CM6646X2 can do.

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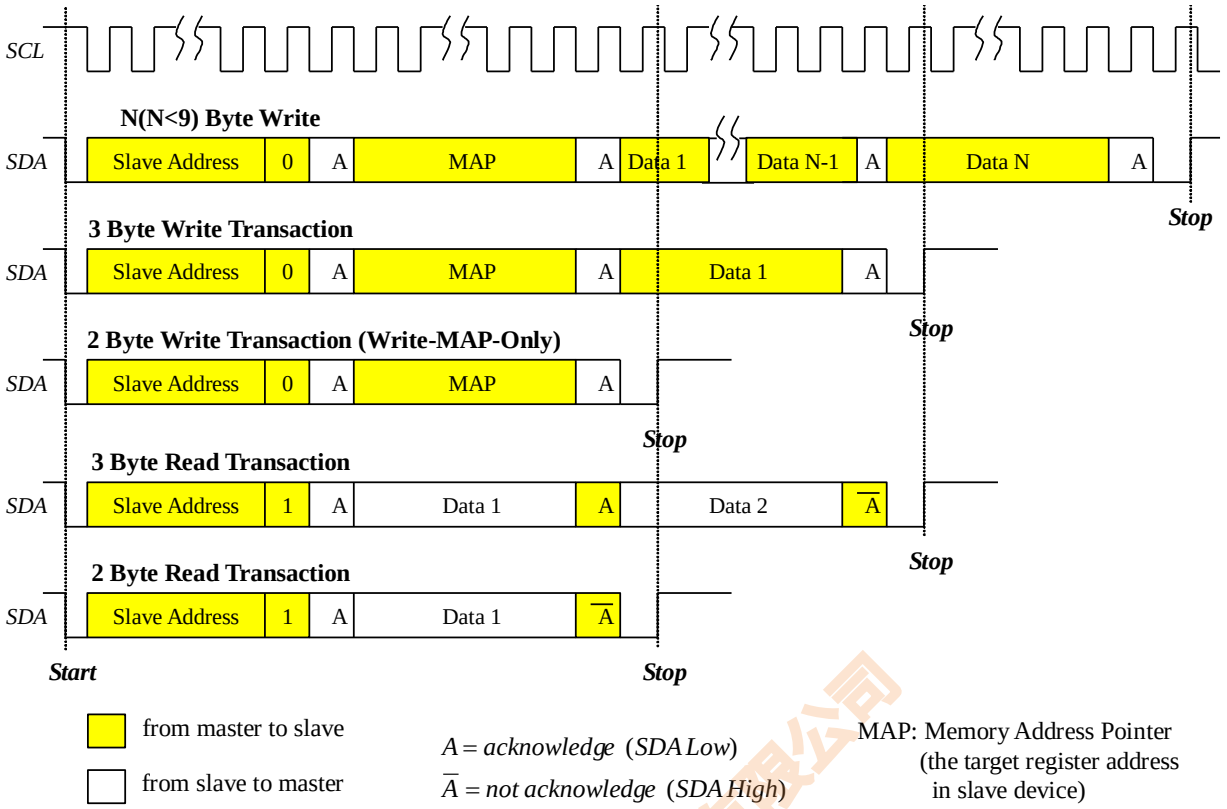

Fig. 6.4.4.2 The 5 basic transactions of the 2-wire master bus supported by the CM6646X2.

In a read transaction, usually the slave device returns the data of the register whose address is in the MAP. If the read transaction is a 3 byte read transaction, the second returned byte is the data in the (address+1) register. Therefore, the action of obtaining the data in slave device is composed of two transactions, namely a 2 byte write transaction (Write-MAP-Only) followed by a read transaction. For the convenience of users, we have designed an auto read transaction, shown in Fig. 6.4.4.3, which is actually the combination of a write and a read transactions.

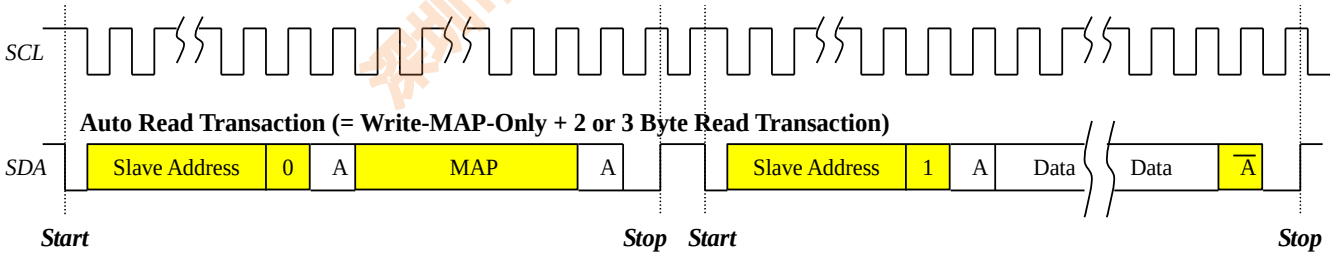

Fig. 6.4.4.3 Auto read transaction in the CM6646X2.

Data transfer with acknowledge is obligatory. The transmitter release SDA line during the acknowledge clock pulse. Then, the receiver must pull down the SDA line during the acknowledge clock pulse so that it remains low for the entire acknowledge clock high period. This is shown in Fig. 6.4.4.4. When a salve does not acknowledge the slave address byte. For example, it is unable to receive or transmit because it is performing some real-time function. The data line should be left high by the slave. The master can then generate either a stop condition to abort the transfer, or a repeated start condition to start a new transfer.

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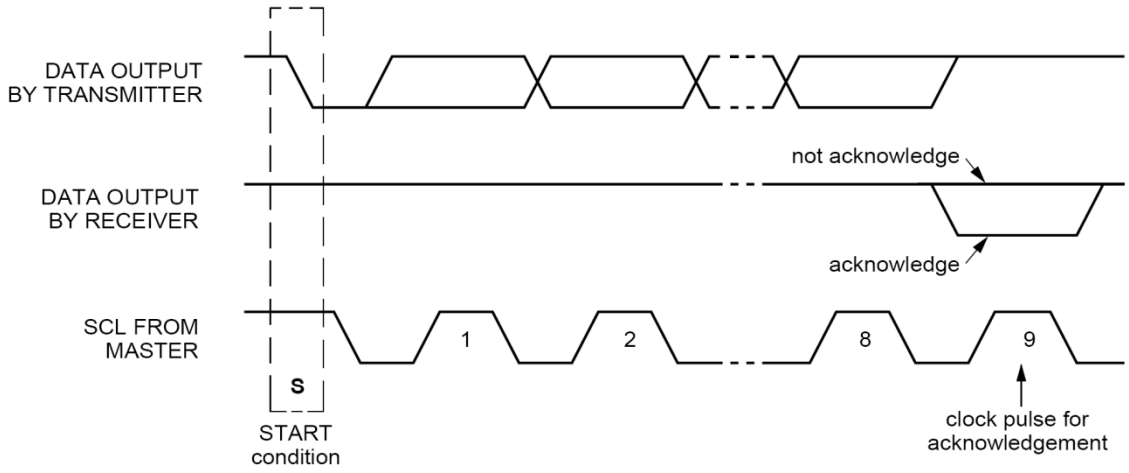

Fig. 6.4.4.4 Acknowledge of the 2-wire bus.

For a read transaction, after the slave address byte is transmitted and acknowledged by slave device, the role of master-transmitter is altered to become master-receiver, and the original slave-receiver is altered to become slave-transmitter. This conception can be easily observed in Fig. 6.4.4.3 and 6.4.4.4, where we use yellow and white blocks to denote the data bit transfer direction. Yellow means the data direction is from the master to the slave. White means the data direction is from the slave to the master. Meanwhile, in a read transaction, the master-receiver must signal the end of the data to the slave transmitter by generating a not-acknowledge ($\overline{A}$) on the last byte that was clocked out of the slave-transmitter. The slave-transmitter should release the SDA line to allow the master to generate a stop or repeated start condition.

6.4.5 Synchronization

The synchronization of the 2-wire bus in the CM6646X2 can be described in two aspects. The first aspect is the synchronization used in arbitration. Although we did not implement arbitration, we did implement clock synchronization. Clock synchronization is used when there are more than two masters connected on the bus. A high to low transition on the *SCL* line will cause the concerned masters start counting the clock low period. Before the clock high state is reached, the masters will hold the *SCL* line in low state. However, the low to high clock transition of one of the masters may not change the state of the *SCL* line if another master's clock is still in low period (because the *SCL* line of the devices are wire-AND connected by open-drain technique). Therefore, the *SCL* line will be held low by the device with the longest clock low period. The other devices with shorter low period, including the CM6646X2, enter a high wait state during this time. Figure 6.4.5.1 listed below is the timing of clock synchronization.

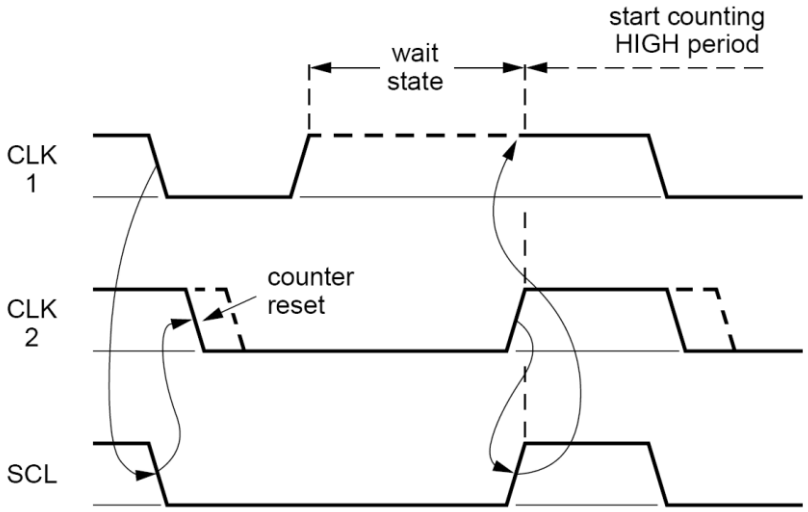

Fig. 6.4.5.1 Clock synchronization for more than two masters in the bus.

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Another aspect of synchronization is the data synchronization between master and slave. If a slave cannot receive or transmit another complete byte of the data until it has performed some other function, for example servicing an internal interrupt or waiting for the driver to prepare the data needed, the salve can hold the clock line *SCL* low to force the master into a wait state. Data transfer then continues when the slave is ready and releases the clock line *SCL*. The data synchronization is shown in Fig. 6.4.5.2.

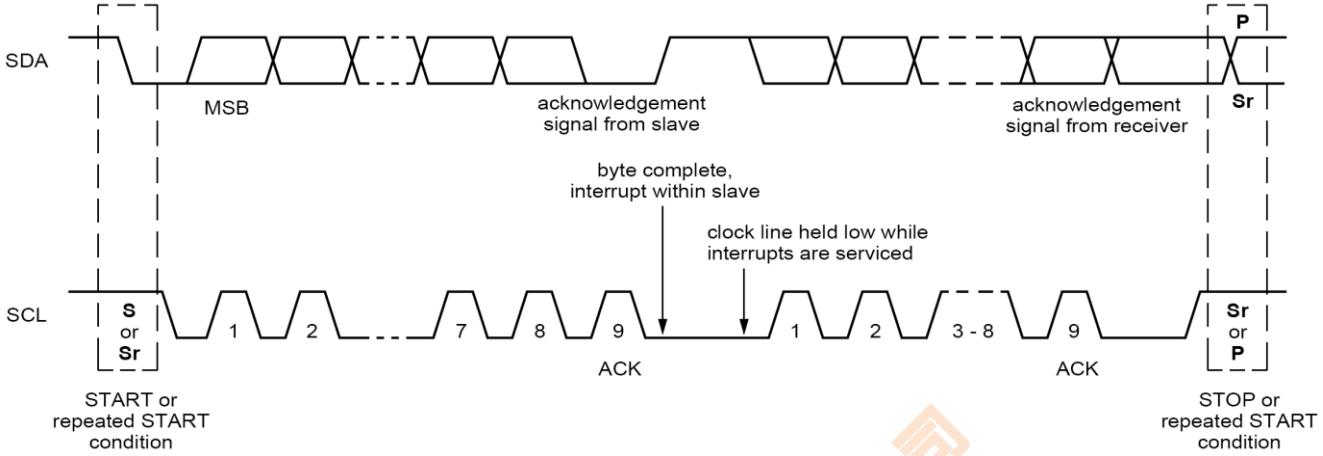

Fig. 6.4.5.2 The data synchronization of the 2-wire master and slave buses in the CM6646X2.

6.4.6 Standard Mode and Fast Mode

Both the 2-wire master and slave buses in the CM6646X2 can support standard mode transfer and fast mode transfer. The data transfer rate of the standard mode is up to 100 Kbits/sec, and the fast mode is up to 400 Kbits/sec. The clock timing of these modes are listed in Fig. 6.4.6.1 and Table 6.4.6.1

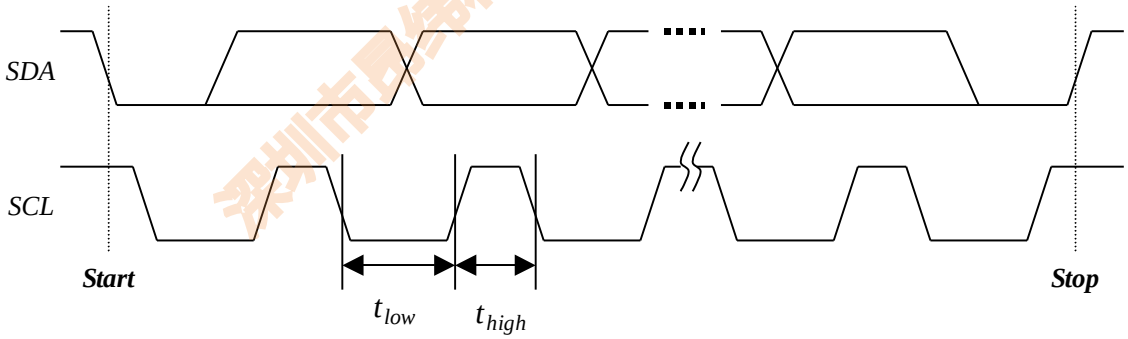

Fig. 6.4.6.1 Standard mode and fast mode timing.

Table 6.4.6.1 Standard mode and fast mode timing.

Parameter	Symbol	Standard mode		Fast mode		Unit
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	KHz
Low period of *SCL* clock	t_{low}	4.8	—	1.3	—	μS
High period of *SCL* clock	t_{high}	4.8	—	0.6	—	μS

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6.5 GPIO

All the GPIO pins can be configured as input or output by the GPIO direction control registers and also can be configure as remote wake up input pin. If they are assigned as outputs, then the contents in the GPIO data registers will be reflected to the corresponding GPIO pins. If they are assigned as inputs, they can be used for jack activity detection. If a speaker is plugged or unplugged, the state of the pin connected with that jack will be changed. As a result, an interrupt is issued to R8051, and an interrupt mask control bit is utilized to decide if the interrupt from that corresponding GPIO pin should be sent. After receiving the interrupt, R8051 must read the GPIO data register (address offset 0x0300h) to discover what pins have changed their states. Then, the R8051 will make some appropriate manipulation in response to the jack activity.

CM6646X2 supports two kinds of Remote-wakeup. One is hardware Remote-wakeup, and the other is software Remote-wakeup. When in Configuration, CM6646X2 has to report the host via the descriptor whether CM6646X2 supports the Remote-wakeup or not. If CM6646X2 reports it supports Remote-wakeup and the host also supports Remote-wakeup, the host will issue the request of Set-feature to enable the Remote-Wakeup feature. If the user selects hardware Remote-wakeup, the user has to select one of the GPIOs to configure as a remote wakeup pin. If there is a transition from 0 to 1 on this pin, that will cause a remote-wakeup to wake up the host from the suspend state. The transition can be from outer world or from the control of the R8051. If the transition is from the control of the R8051, this is called Software Remote-wakeup. Software Remote-wakeup is implemented by the register. If the user selects software Remote-wakeup, the 8051 has to write the register to cause the transition from 0 to 1 to wake up the host.

CM6646X2 has a de-bouncing circuit to filter the interrupt to R8051. There are two options to select which are 16ms and 8ms. The user can select one option to use according to their application.

6.6 I2S Interface

The main audio interface of the CM6646X2 is I2S, which has three clock signals, MCLK, BCLK and LRCK, and at least one data line depending on the channels supported. One data line contains two channels. The three I2S clock symbols are explained below.

MCLK = main clock.
BCLK = bit clock.
LRCK = left and right clock.

6.6.1 The Basics of I2S Bus

Both master and slave modes of I2S are supported by the I2S interfaces of the CM6646X2, namely I2S DAC, I2S ADC. Master mode means BCLK and LRCK are provided by the CM6646X2 as shown in Fig. 6.6.1.1(a). On the contrary, slave mode means BCLK and LRCK are provided by the I2S codecs as depicted in Fig. 6.6.1.1(b).

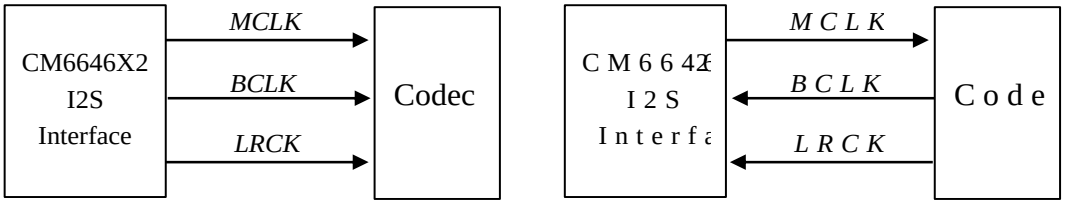

Fig. 6.6.1.1 (a) Master mode; (b) Slave mode.

Fig. 6.6.1.2 indicates the basic waveform of I2S. Note that BCLK is generated at the positive edges of MCLK with the ratios 1, 1/2, 1/4, or 1/8, and LRCK is generated at the negative edges of BCLK with the ratios 1/64, 1/128, 1/256. Data bits are transited at the negative edges of BCLK, and are sampled at the positive edges of BCLK. In case of playback, CM6646X2 is the data transmitter and the codec is the data receiver. As for recording, the roles of CM6646X2 and codec are reversed.

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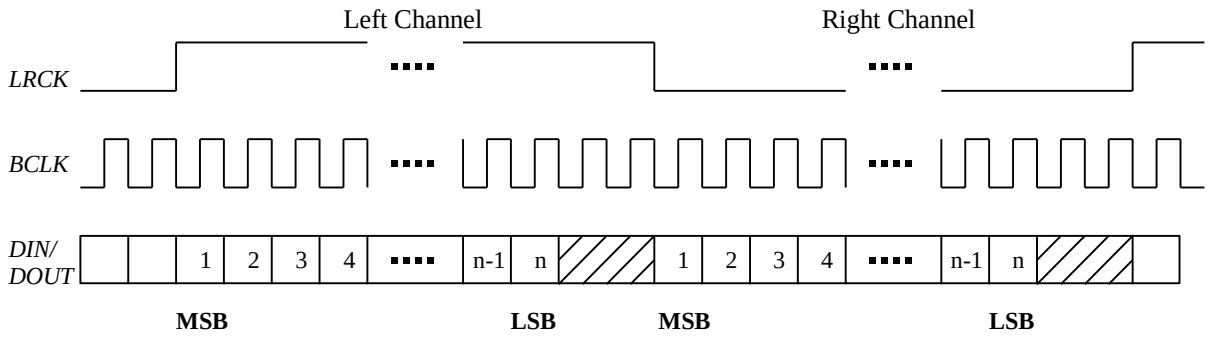

Fig. 6.6.1.2 The basic timing diagram of the I2S interface.

For the I2S DAC controller, the audio data is transformed from the parallel format to the serial format before transmitted. Then, the bit data is shifted out one by one with the MSB first via DOUT signal. If the I2S DAC controller is set to 32 bits, at least 32 BCLK clocks must exist in both LRCK left and right channels. In the same manner, the audio data is transformed from the coming serial format to the parallel format for a I2S ADC controller.

6.6.2 LJ Mode

In the LJ mode of the I2S DAC controller, the MSB data bit is clocked out by the CM6646X2 at the negative edge of BCLK which is aligned to the transition of LRCK. In the LJ mode of I2S ADC controllers, the MSB data bit is clocked out by codecs and sampled by the CM6646X2 at the first positive edge of BCLK which follows a LRCK transition. LRCK is high during left channel transmission and low during right channel transmission in the LJ mode. Fig. 6.6.2.1 shows all of these.

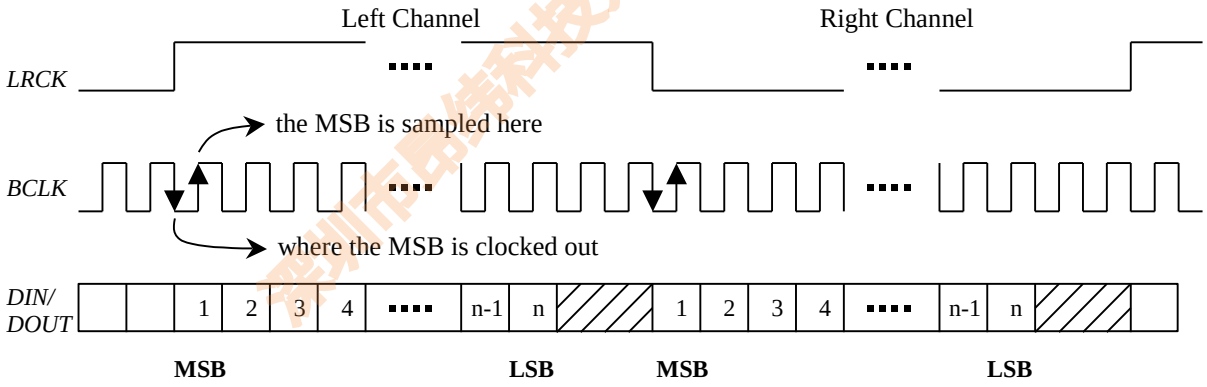

Fig. 6.6.2.1 LJ mode timing diagram of I2S interface.

6.6.3 I2S Mode

In the I2S mode of the I2S DAC controller, the MSB data bit is clocked out by CM6646X2 at the first negative edge of BCLK which follows a LRCK transition. In the I2S mode of I2S ADC controllers, the MSB data bit is clocked out by codecs and sampled by the CM6646X2 at the second positive edge of BCLK which follows a LRCK transition. LRCK is low during left channel transmission and high during right channel transmission in the I2S mode. Fig. 6.6.3.1 indicates all of these.

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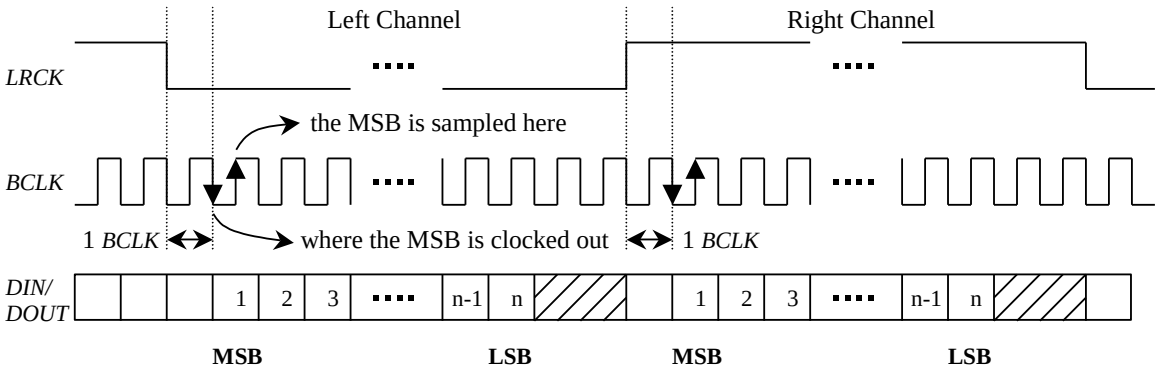

Fig. 6.6.3.1 I2S mode timing diagram of I2S interface.

6.6.4 The I2S Clock Generation

The clock generation of I2S controllers is very complicated, so we use the block diagram in Fig. 6.6.4.1 to roughly present how the clocks are generated.

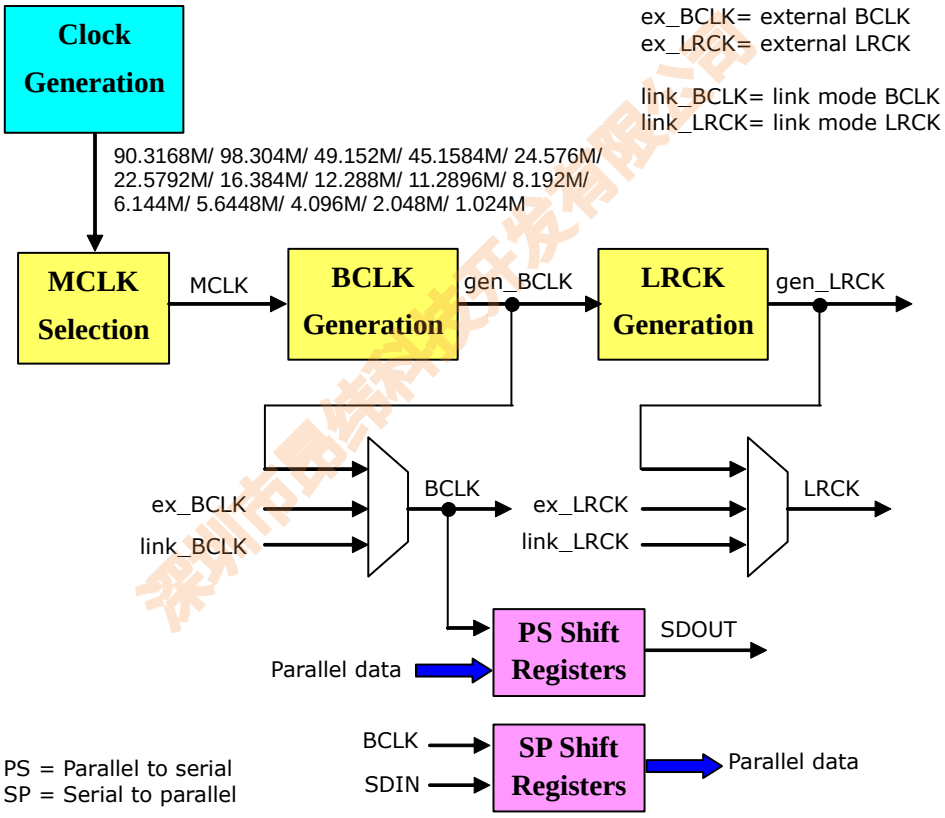

Fig. 6.6.4.1 I2S clock generation block.

The I2S clock switching is also very important, because the glitches occurred at clock switching in multiplexers 1 and 2 can evoke serious timing errors in BCLK, LRCK counter blocks, and serial to parallel receiver or parallel to serial transmitter blocks when post simulating is performing. Therefore, state machines, not shown in Fig. 6.6.4.1, are used to control the clock switching.

Table 6.6.4.1 gives the actual MCLK frequency which is a function of sampling rate and MCLK/LRCK ratio. Table 6.6.4.2 indicates the BCLK frequency which is a function of MCLK/LRCK ratio and BCLK/LRCK ratio. The BCLK frequency is expressed as an MCLK equation. The LRCK is shown in Table 6.6.4.3. It is equal to sampling rate.

Table 6.6.4.1 The MCLK frequency as a function of sampling rate and MCLK/LRCK ratio.

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Sampling rate	mclk/lrck ratio		
	128	256	512
8kHz	1.024MHz	2.048MHz	4.096MHz
16kHz	2.048MHz	4.096MHz	8.192MHz
32kHz	4.096MHz	8.192MHz	16.384MHz
44.1kHz	5.6448MHz	11.2896MHz	22.5792MHz
48kHz	6.144MHz	12.288MHz	24.576MHz
64kHz	8.192MHz	16.384MHz	---
88.2kHz	11.2896MHz	22.5792MHz	45.1584MHz
96kHz	12.288MHz	24.576MHz	49.152MHz
176.4kHz	22.5792MHz	45.1584MHz	90.3168MHz
192kHz	24.576MHz	49.152MHz	98.304MHz

Sampling rate	mclk/lrck ratio	
	64	128
352.8kHz	22.5792MHz	45.1584MHz
384kHz	24.576MHz	49.152MHz
705.6kHz	45.1584MHz	90.3168MHz
768kHz	49.152MHz	98.304MHz
48kHz	6.144MHz	12.288MHz
64kHz	8.192MHz	16.384MHz
88.2kHz	11.2896MHz	22.5792MHz
96kHz	12.288MHz	24.576MHz
176.4kHz	22.5792MHz	45.1584MHz
192kHz	24.576MHz	49.152MHz

Table 6.6.4.2 The BCLK frequency as a function of BCLK/LRCK ratio and MCLK/LRCK ratio.

mclk/lrck ratio	bclk/lrck ratio		
	64	128	256
128	bclk = mclk/2	bclk = mclk	---
256	bclk = mclk/4	bclk = mclk/2	bclk = mclk
512	bclk = mclk/8	bclk = mclk/4	bclk = mclk/2

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Table 6.6.4.3 The LRCK frequency is equal to sampling rate.

Sampling rate	lrck
8kHz	8kHz
16kHz	16kHz
32kHz	32kHz
44.1 kHz	44.1 kHz
48 kHz	48 kHz
64 kHz	64 kHz
88.2 kHz	88.2 kHz
96 kHz	96 kHz
176.4 kHz	176.4 kHz
192 kHz	192 kHz

6.6.5 I2S Serial to Parallel Data Receiver and Parallel to Serial Data Transmitter

Basically, the transmitter and receiver are shift registers. The major difference of them is that receiver is operated on the rising edge of BCLK and transmitter is operated on the falling edge of BCLK. The important design of the two blocks that are worthy of mention is the timing when the load signals of the shift registers should be created. There are two load signals in the transmitter and receiver. The load signal used in master mode is called master_load, and the load signal used in slave mode is called slave_load. The timing of the two load signals are shown in Fig. 6.6.5.1.

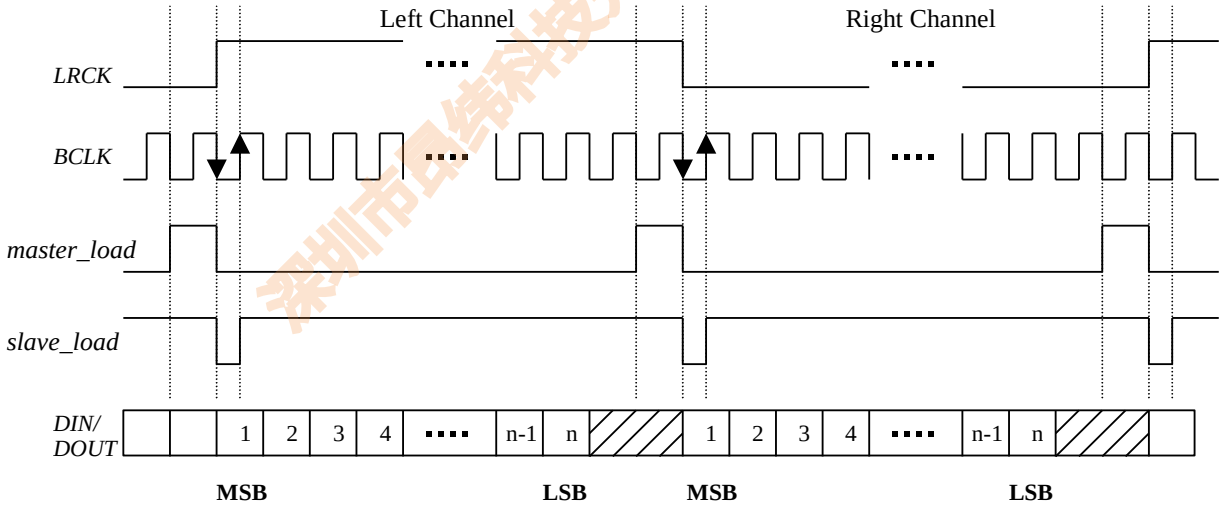

Fig. 6.6.5.1 The timing of load signal in I2S transmitter and receiver

Next, we will explain why the load signals are different in master and slave modes. In the master mode, the CM6646X2 dominates the creation of BCLK. It can decide how many BCLK's exist in an LRCK left/right channel, so the CM6646X2 is able to issue load signal just before the transition (low to high or high to low) of LRCK to load new audio data into the shift registers to meet the subsequent MSB transmission in time. However, in the slave mode, codecs dominate the generation of BCLK. The CM6646X2 does not know how many BCLK's exist in an LRCK left/right channel, and when it should generate the load signal Those messages are only known by I2S master. As a result, in order to make the CM6646X2 be able to work with all kinds of I2S masters in slave mode, an asynchronous salve_load is

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created to load new audio data into the shift registers. The salve_load signal is derived from the transition edge of LRCK. No more information is needed in advance for the CM6646X2 I2S slave mode. That makes it universal.

7. Xear™ Sound Processing

Xear™ is the core name of C-Media sound effect technology; it includes audio and voice processing. These sections describe the main sound processing on CM6646X2.

7.1 Xear 3D Sound Anchor

The new 3D Sound Anchor sound effect adds a new HRTF, and the extended space effect is 3D panoramic space, which has more processing methods for the upper and lower spaces, increasing the sense of three-dimensional and space

7.2 Xear™ Surround Headphone

Xear™ Surround Headphone creates a realistic 5.1/7.1CH surround sound field over stereo headphones. Combined with Surround sound in games, gamers could enjoy amazing 3D gaming sound experience and combat advantages. It also delivers natural sound space for stereo music as real as playback on speakers for longer listening on headphones without fatigue.

Xear Surround Headphone provides music/gaming and movie modes for different applications. User can switch the surround mode to get the best effect in different situation.

7.3 Xear™ Software 10 Band Equalizer

It provides 10-band EQ function, User will able to adjust the EQ band by manual and create customize preset items or click on the preset EQ mode. There are 12 preset modes such as Bass, Treble, Live, Rock, Jazz, etc.

7.4 Xear™ Audio Brilliant

Xear™ Audio Brilliant restores the clarity and details of compressed audio in music, movies and games (MP3, WMA, AAC, AC3, etc.). Make the sound more dynamic and brilliant. Audio compression algorithms will usually sacrifice some audio frequency signals. It might result in flat, thin, and lifeless sounds. Audio Brilliant recreates the subtleties of the original performance.

7.5 Xear™ Dynamic Bass

Xear™ Dynamic Bass reproduces the deep and vibrating bass in music, games, and movies, and music even over small speaker/headphone drivers and enclosures. Applying psychoacoustic techniques to make users feel stronger bass signals of drums, bass guitars, explosions, automobile engines, etc.

It can overcome small speaker driver's poor bass limitation without damage.

7.6 Xear™ Voice Clarity

Xear™ Voice Clarity can increase the clarity, intelligibility, and prominence of receiving voice in games, VOIP, music, or movies without suppressing or changing other background audio. Adjustable voice clarity levels make you hear the voice more clearly or learn language more easily. Optional background stationary noise suppression in communication simultaneously.

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7.7 Xear™ Smart Volume

Xear™ Smart Volume normalizes sound levels of music, Internet AV clips, and movies to reduce the probabilities that require volume adjustments on Docking Speakers and PCs.

7.8 Xear™ Magic Voice

Xear™ Magic Voice is a great feature for disguising your voice (using cartoon/monster/male/female effects) for VOIP and online gaming Applications.

7.9 Xear™ AI Noise Cancellation

Xear™ AI Noise Reduction (AI NR) is different from traditional noise reduction, the traditional noise reduction only can reduce noise on the waveform for fixed frequency noise, AI Noise Reduction through neural network learning can distinguish between human voices and environmental noises (such as crying babies, pets, environmental noise, etc.). In addition, AI Noise Reduction also supports the noise reduction of the sound playback device, so the listener can hear the voice of the other party or the speaker more clearly.

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ	Max.	Unit
Storge temperature	T_S	-40	-	125	°C
Digital supply voltage	XD5V_XA5V	-	-	5.5	V
ESD (Body mode)	HBM	-	±4000	-	V
ESD (Machine mode)	MM	-	±200	-	V

8.2 Recommended Operation Conditions

Parameter	Symbol	Min.	Typ	Max.	Units
Operating ambient temperature	T_A	-40	25	85	°C
Supply voltage	XD5V_XA5V	4.085	4.3	4.515	V
Digital Core	VCC12	1.08	1.2	1.32	V

8.3 Power Consumption

Test Conditions: XD5V_XA5V = 4.3V, AGND =0V, T_A =+25°C, MCU Clock = 6MHz.
Sample Rate=48kHz, 24Bits, Operation: Headphone output, Microphone input,
Volume setting = Gain 0dB

Parameter	Symbol	Min.	Typ	Max.	Units
Total power consumption (Playback + Record)	-	-	53	-	mA
Standby power consumption	-	-	52.8	-	mA
Suspend mode power consumption	-	-	1.62	-	mA

8.4 DC Characteristics

Test Conditions: XD5V_XA5V = 4.3V, AGND =0V, T_A =+25°C

Parameter	Symbol	Min.	Typ	Max.	Units
Input voltage range	DI	0	-	3.6	V
Output voltage rage	DO	0	-	3.6	V
High-level input voltage	Vih	2.0	-	-	V
Low-level input voltage	Vil	-	-	0.8	V

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High-level output voltage	Voh	2.4	-	-	V
Low-level output voltage	Vol	-	-	0.4	V

Analog I/O Characteristics

Parameter	Symbol	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max		
Microphone Input Impedance	MII	MIC IN	-	20	-	kΩ	
Microphone A-A Input Impedance	MAII	MIC IN	-	20	-	kΩ	Mic Gain=0dB
Microphone Bias Open Circuit Voltage	VMICBIAS	MICBIAS	2.7	3	3.3	V	
Microphone Bias Output Current	IMICBIAS	MICBIAS	-	-	1.25	mA	RMIN=2.2kΩ
Microphone Bias Output Impedance	ROUTMICB	MICBIAS	600	650	700	Ω	
Power Supply Rejection Ratio (PSRR) for Microphone Bias	PSRRMICB	MICBIAS	-	100	-	dB	Internal regulators active, at maximum load current (0.5 mA), 1 kHz sine wave at 1 Vrms

9. Analog Performance

9.1 DAC audio quality

T_A =25℃, XD5V_XA5V = 4.3V, AGND =0V, Equalizer disable, and list others might impact quality
Hardware rev: CM6646X2_Demoboard_V100
Firmware rev: CM6646X2-Demoboard-0206
Test Platform: ASUS NB Intel I7-6700HQ, 16G RAM, Windows 11/64bit
Test AP: AP525B
Ch1=L CH ; Ch2=R CH

Items	Test Conditions		Test Values			Unit
			Min.	Typ.	Max.	
Full Scale Output Voltage	10KΩ loading		-	1040	-	mVrms
	32Ω loading		-	880	-	mVrms
	32Ω with 33Ω cascade loading Note 1		-	460	-	mVrms
Noise Level	10KΩ loading		-	-95.9	-	dB
	32Ω loading		-	-97.4	-	dB
	32Ω with 33Ω cascade loading		-	-103.3	-	dB
THD + N -3dBFS@1KHz	10KΩ Loading Figure 1	48K/24bits	-	-89.9	-	dBFS

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	32Ω Loading Figure 2		-	-74.3	-	dBFS
	32Ω with 33Ω cascade loading Figure 3		-	-81.4	-	dBFS
Dynamic Range With A-Weighted, test by -60dBFS 1K sine wave	10KΩ Loading	48K/24bits	-	96.2	-	dBFS
	32Ω loading	48K/24bits	-	96.2	-	dBFS
	32Ω with 33Ω cascade loading	48K/24bits	-	96.2	-	dBFS
SNR (Noise level during active) With A-Weighted, test by -96dBFS 1K sine wave	10KΩ loading	48K/24bits	-	96.1	-	dBFS
	32Ω loading	48K/24bits	-	96.1	-	dBFS
	32Ω with 33Ω cascade loading	48K/24bits	-	96.2	-	dBFS
Cross-talk 20Hz ~ 20KHz	10KΩ loading Figure 4	48K/24bits	-	-107.1 (1KHz)	-	dBFS
	32Ω loading Figure 5	48K/24bits	-	-76.4 (1KHz)	-	dBFS
	32Ω with 33Ω cascade loading Figure 6	48K/24bits	-	-81.8 (1KHz)	-	dBFS
Frequency Response	10KΩ loading Figure 7	48K/24bits	0.066 (20Hz)	-	-0.962 (20KHz)	dB
	32Ω loading Figure 8	48K/24bits	0.67 (20Hz)	-	-0.962 (20KHz)	dB
	32Ω with 33Ω cascade loading Figure 9	48K/24bits	0.064 (20Hz)	-	-0.967 (20KHz)	dB

Note 1: Headphone 32 ohm loading audio quality measure by cascading 33 or 0 ohm resistors, the schematic diagram as below.

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THD+N @ 10KΩ loading

Figure 1

THD+N @ 32Ω loading

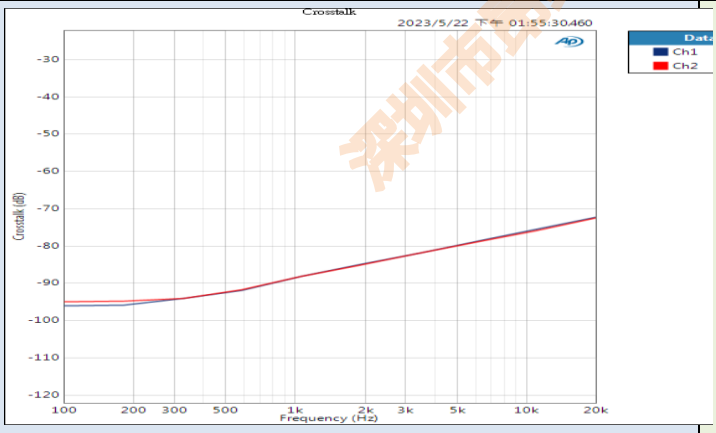
Figure 2

THD+N @ 32Ω with 33Ω cascade loading

Figure 3

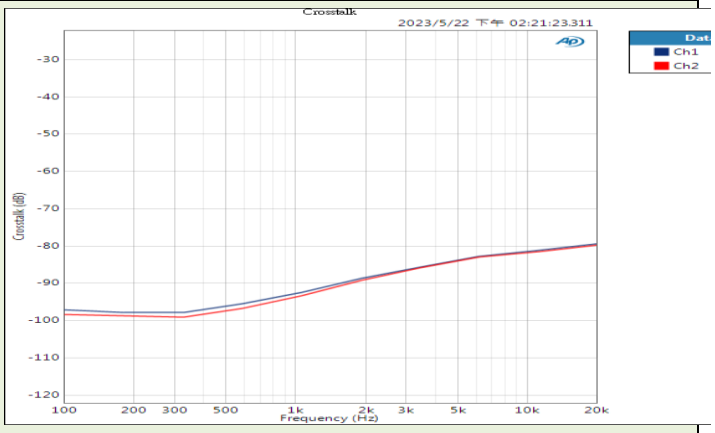
Cross-talk @ 10KΩ loading

Figure 4



Cross-talk @ 32Ω loading

Figure 5



Cross-talk @ 32Ω with 33Ω cascade loading

Figure 6

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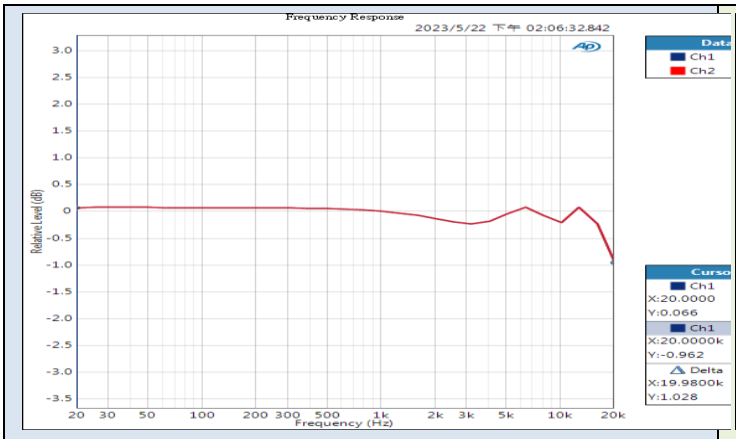

Frequency Response @ 10KΩ loading

Figure 7

Frequency Response @ 32Ω loading

Figure 8

Frequency Response @ 32Ω with 33Ω cascade loading

Figure 9

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9.2 ADC audio quality

T_A =25℃, XD5V_XA5V = 4.3V, AGND =0V, 997Hz Sine-wave, measure bandwidth is 20Hz to 20kHz, Equalizer disable, AGC off, Mic Gain= 0dB,
Hardware rev: CM6646X2_Demoboard_V100
Firmware rev: CM6646X2-Demoboard-0206
Test Platform: ASUS NB Intel I7-6700HQ, 16G RAM, Windows 11/64bit
Test AP: AP525B

Items	Test Conditions		Test Values			Unit
			Min.	Typ.	Max.	
Full Scale Input Voltage	0dB Gain	48K/24bits	-	780	-	mVrms
Microphone Input Impedance	A-A Disable		-	20	-	K Ω
	With-A-A, Note 2		-	10	-	
THD+N With None Filter (1KHZ)	0dB Gain Figure 10	48K/24bits	-	-89.8	-	dB
	20dB Gain Figure 11	48K/24bits	-	-83.9	-	dB
Dynamic Range With A-Weighted, test by -60dBFS 1K sine wave	0dB Gain	48K/24bits	-	-94.7	-	dB
	20dB Gain	48K/24bits	-	-88.3	-	dB
SNR (Noise level during active) With A-Weighted, test by -96dBFS 1K sine wave	0dB Gain	48K/24bits	-	94.8	-	dB
	20dB Gain	48K/24bits	-	88.3	-	dB
Sampling Frequency Accuracy	0dB Gain	48K/24bits	-	0.0162	-	%
	20dB Gain	48K/24bits	-	0.0164	-	%

Note 2: A-A stands for Analog to Analog, it is Microphone input directly out to Headphone.

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Cross-talk	Sampling frequency		100	-	10K	HZ
	0dB Gain Figure 12	48K/24bits	-	-100.3 (1KHz)	-	dB
	20dB Gain Figure 13	48K/24bits	-	-95.5 (1KHz)	-	dB
Frequency Response (ref.:-20dB)	Band Edge		20	-	20K	HZ
	0dB Gain Figure 14	48K/24bits	-1.14	-	-0.774	dB
	20dB Gain Figure 15	48K/24bits	-1.138	-	-0.796	dB

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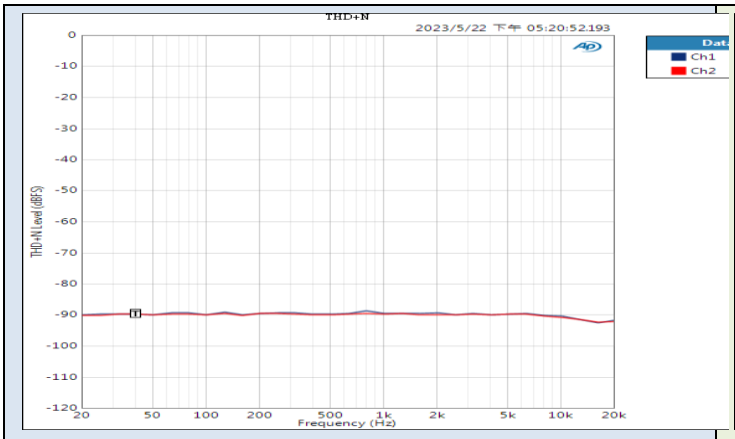
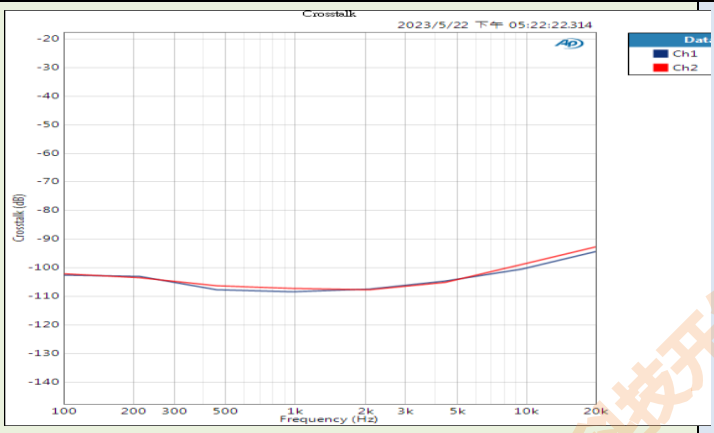


THD+N 0dB Gain

Figure 10

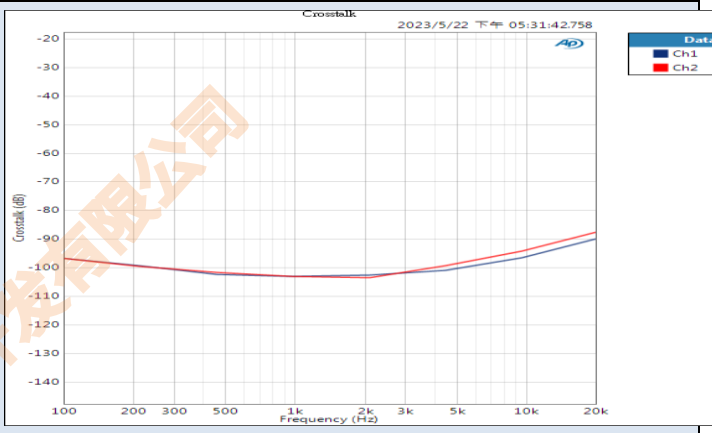
THD+N 20dB Gain

Figure 11



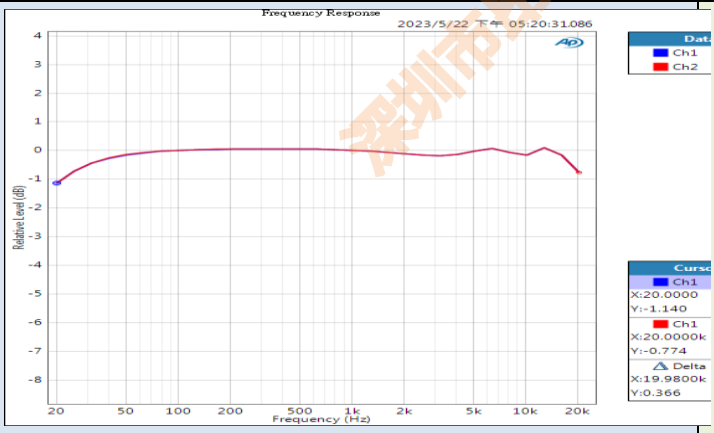
Cross-talk 0dB Gain

Figure 12



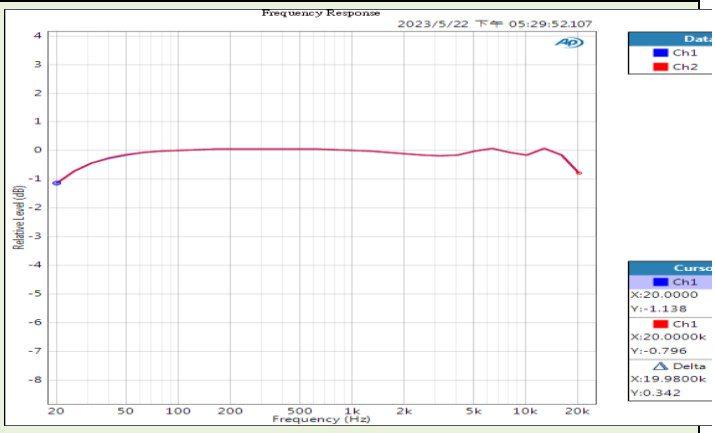
Cross-talk 20dB Gain

Figure 13



Frequency Response 0dB Gain

Figure 14



Frequency Response 20dB Gain

Figure 15

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9.3 Analog Monitoring / Side tone (A-A) path audio quality

T_A=25℃, XD5V_XA5V = 4.3V, AGND =0V, Microphone-In to Headphone-Out, Master Volume=0dB, Mic Gain=0dB, Fs/Bit-depth=48KHz/24bit
Hardware rev: CM6646X2_Demoboard_V100
Firmware rev: CM6646X2-Demoboard-0206
Test Platform: ASUS NB Intel I7-6700HQ, 16G RAM, Windows 11/64bit
Test AP: AP525B

Items	Test Conditions	Test Values			Unit
		Min.	Typ.	Max.	
Full Scale Output Voltage	10KΩ loading	-	1027	-	mVrms
	32Ω loading	-	876	-	
	32Ω with 33Ω cascade loading	-	464	-	
THD + N -3dBFS@1KHz	10KΩ loading Figure 16	-	-86.7	-	dB
	32Ω loading Figure 17	-	-69.6	-	dB
	32Ω with 33Ω cascade loading Figure 18	-	-76.9	-	dB
Dynamic Range With A-Weighted, test by -60dBFS 1K sine wave	10KΩ loading	-	-92.7	-	dB
	32Ω loading	-	-92.7	-	
	32Ω with 33Ω cascade loading	-	-92.1	-	
SNR (Noise level during active) With A-Weighted, test by -96dBFS 1K sine wave	10KΩ loading	-	-92.8	-	dB
	32Ω loading	-	-92.8	-	
	32Ω with 33Ω cascade loading	-	-92.1	-	
Cross-talk	Sampling frequency	-	1K	-	HZ
	10KΩ loading Figure 19	-	-91.9	-	dB
	32Ω loading Figure 20	-	-67	-	
	32Ω with 33Ω cascade loading Figure 21	-	-71.2	-	
Frequency Response (ref.:-20dB)	Band Edge	20	-	20K	HZ
	10KΩ loading Figure 22	-1.978	-	-0.01	dB
	32Ω loading Figure 23	-1.985	-	-0.01	
	32Ω with 33Ω cascade loading Figure 24	-1.992	-	0	
Sampling Frequency Accuracy	10KΩ loading	-	0.0001	-	%
	32Ω loading	-	0.0001	-	
	32Ω with 33Ω cascade loading	-	0.0001	-	

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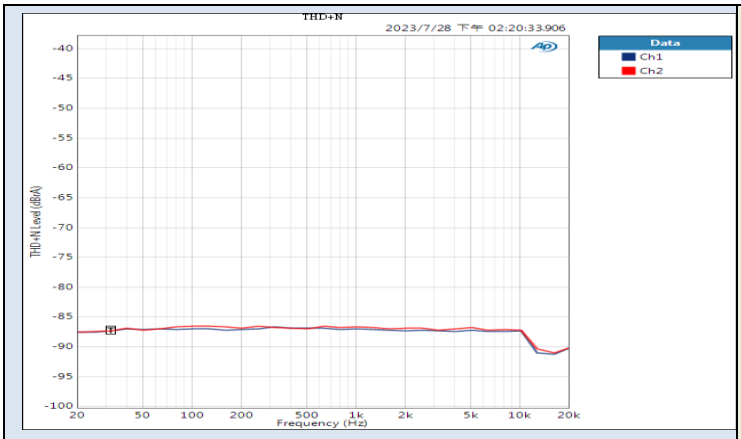
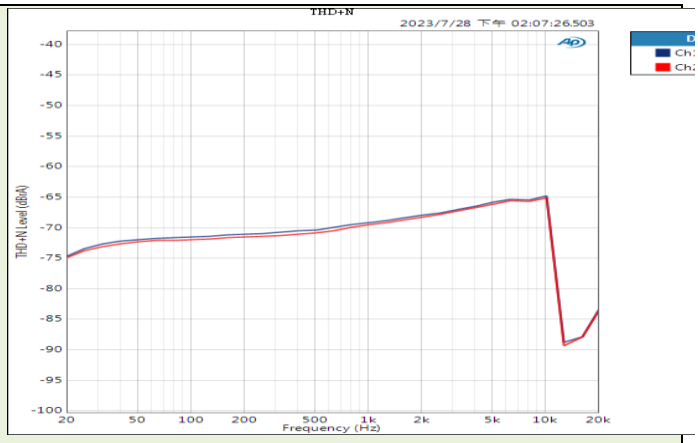


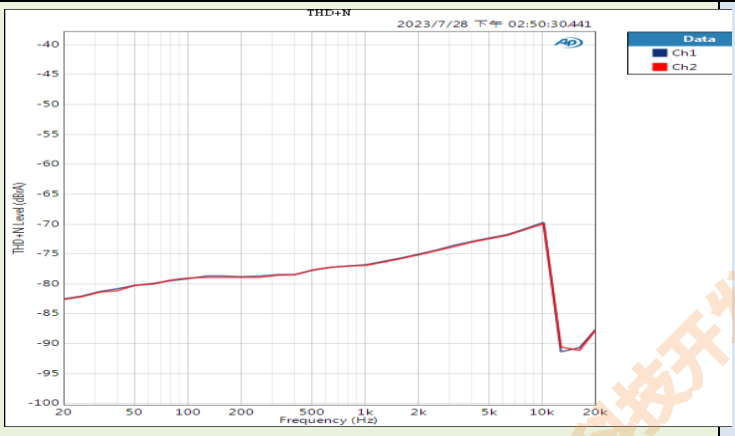
THD+N @ 10KΩ loading

Figure 16



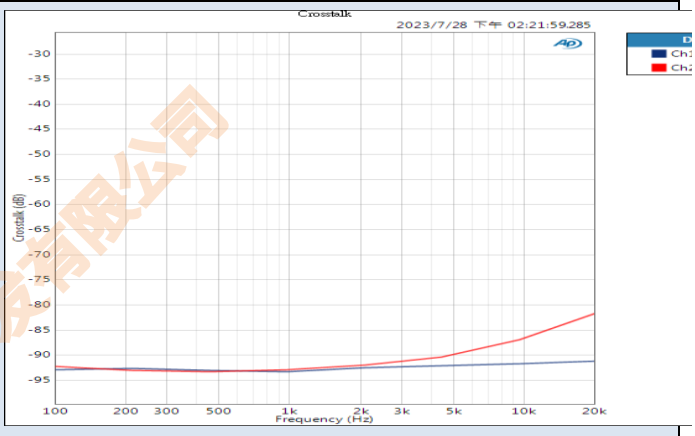
THD+N @ 32Ω loading

Figure 17



THD+N @ 32Ω with 33Ω cascade loading

Figure 18



Cross-talk @ 10KΩ loading

Figure 19

Cross-talk @ 32Ω loading

Figure 20

Cross-talk @ 32Ω with 33Ω cascade loading

Figure 21

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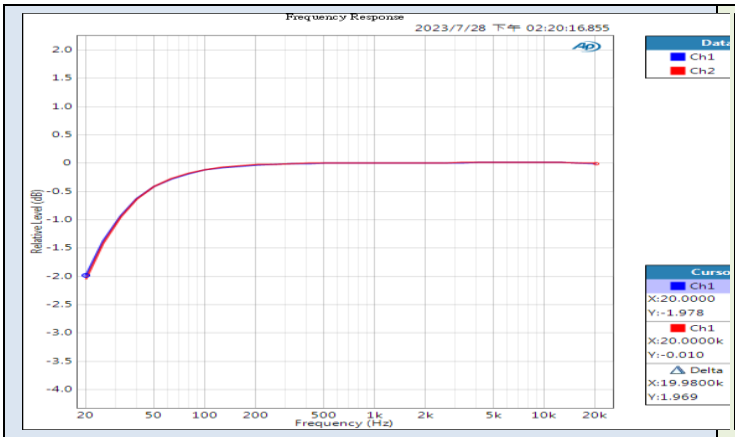
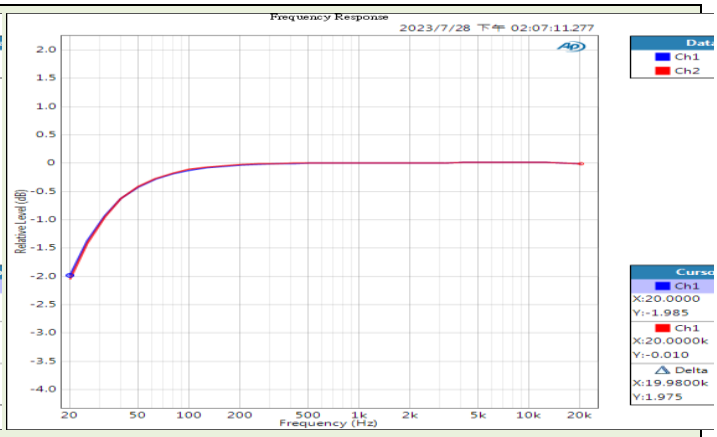


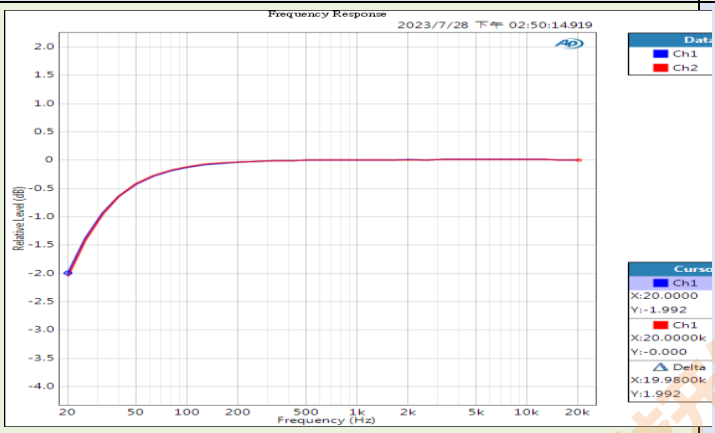
Frequency Response @ 10KΩ loading

Figure 22



Frequency Response @ 32Ω loading

Figure 23



Frequency Response @ 32Ω with 33Ω cascade loading

Figure 24

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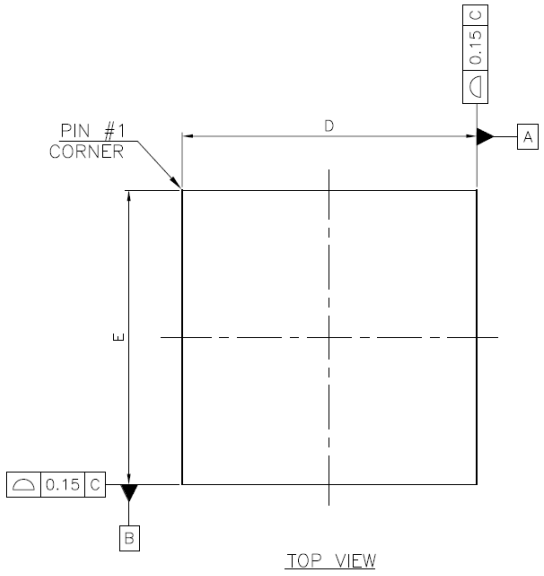
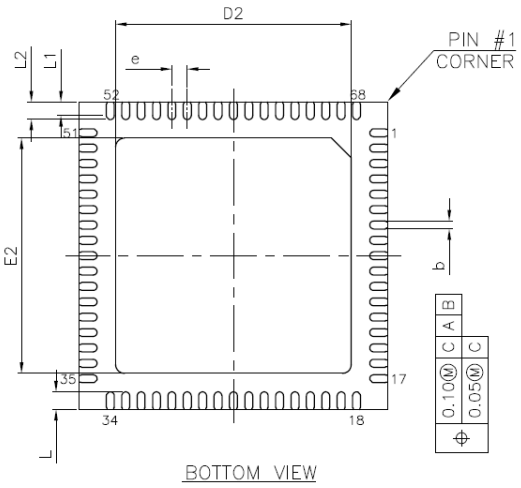
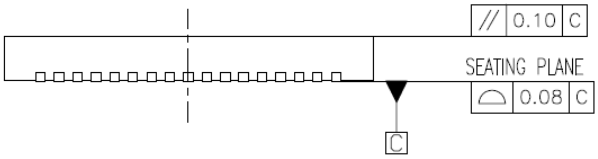
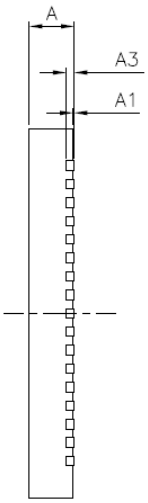
10. Package Dimensions

QFN68 7mm x 7mm









	SYMBOL	MIN.	NOM	MAX.	MIN.	NOM	MAX.
Total thickness	A	0.80	0.85	0.90	0.75	0.80	0.85
Standoff	A1	0.00	0.02	0.05	0.00	0.02	0.05
Lead thickness	A3	0.15 REF.			0.15 REF.		
Body size	D	6.90	7.00	7.10	6.90	7.00	7.10
	E	6.90	7.00	7.10	6.90	7.00	7.10

BBD no	Pad size	Lead width b			Exposed pad width D2			Exposed pad length E2			Lead pitch e			Lead length L			L1			L2			LEAD FINISH	
		MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	Pure Tin	PPF
	231x231 MIL	0.13	0.18	0.23	5.26	5.36	5.46	5.26	5.36	5.46	0.35 BSC			0.35	0.40	0.45	--	0.31	--	--	0.39	--	V	X

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— End of Datasheet —

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