

[illegible]

The schematic diagram illustrates the HP VC Mode circuit. It features two input lines, HP_L and HP_R, each with a 0Ω resistor (R3, R6) and a 10nF capacitor (C2, C3) to ground. These lines pass through 100nF capacitors (L2, L3) and then through diodes D2 and D3 to a common node. This node is connected to a 100nF capacitor (C4) and a 10kΩ resistor (R4) to ground. The output of the circuit is connected to a CPU D3048A via a J2 connector. The output lines are labeled HPL, HPR, VC_HP, and MCP.

Wiring diagram for the FN_MHVO_6 terminal block:

- Terminal R40 (0) is connected to AVOL_VR.
- Terminal R41 (NC 0) is connected to AVOL_ENCV.
- Terminal R42 (NC 0) is connected to Buttons.
- Terminal R44 (NC 0) is connected to MIC_IN-.

R15 for HID1/HID2/HID3 key

2026/01/09 SCH review
C9 changed from 105 to 104

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