DESCRIPTION

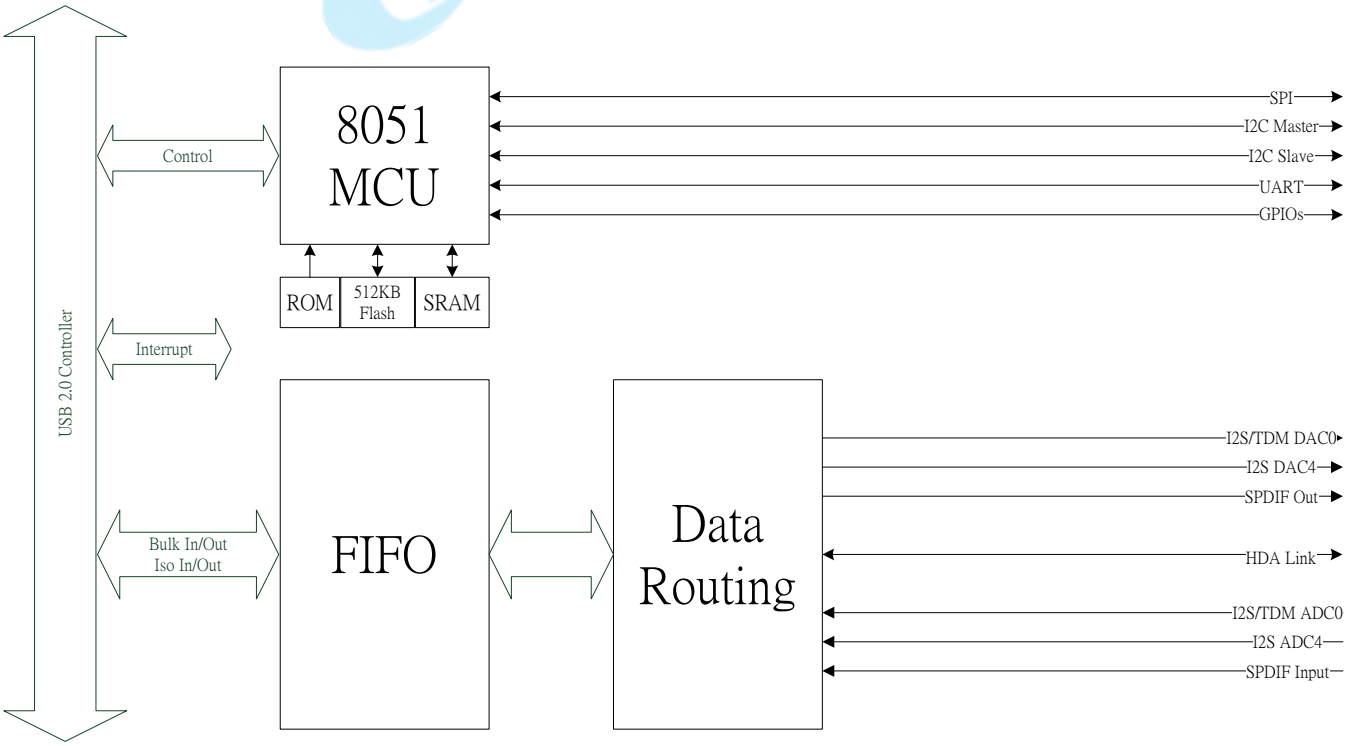
The CM6212 is a USB 2.0 high-speed audio processor that supports USB Audio Device Class 1.0 and 2.0. The CM6212 provides standard HDA, I2S TDM and S/PDIF digital audio interface. The maximum outputs are 12 channels with 8 channels TDM, 2 channels I2S and 2 channels S/PDIF and the maximum inputs are 12 channels with 8 channels TDM, 2 channels I2S and 2 channels S/PDIF. Moreover, the CM6212 supports I2C, SPI and GPIOs to communicate with external device.

The CM6212 is embedded with 8051 MCU and 512KB flash makes it is very flexible to change the USB topology or communicate with external device by changing internal flash code. It also integrates two tricolor PWM LED drivers for status indication.

FEATURES

- USB specification 2.0 full-speed/high speed-compatible
- USB audio device class 1.0/2.0-compatible
- USB human interface device (HID) class 1.1-compliant
- Supports USB suspend/resume/reset functions
- Supports control, interrupt, bulk, and isochronous data transfers
- 2 stereo I2S serial audio output/input interfaces
- The first I2S output/input supports TDM interface
- S/PDIF input and output up to 192K/24bits
- Support HDA link interface for HDA codec
- 1 I2C master, 1 I2C slave, 3 SPI master, 18 GPIOs
- Integrate two tricolor PWM LED drivers

BLOCK DIAGRAM



Release notes

Revision	Date	Description
0.93	2019/03/06	- Draft release
0.94	2019/08/20	- Typo correction
0.95	2020/04/06	- Modify 3.2 and 7.2
1.0	2020/04/21	- Formal release
1.1	2020/08/19	- Modify Table 1 - Add Table 2
1.21	2021/06/09	- Modify 7.Electrical Characteristics - Modify pin description
1.30	2022/02/08	- Remove 8K/16K/32K/64KHz sample rate from I2S interface - Remove 64K sample rate from SPDIF interface
1.40	2025/07/02	- Modify Electrical Characteristics

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1 Description and Overview

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The CM6212 is embedded with 8051 MCU and 512KB flash makes it is very flexible to change the USB topology or communicate with external device by changing internal flash code. It also integrates two tricolor PWM LED drivers for status indication.

2 Ordering Information

Product	Package Marking	Package Type	Transport Media
CM6212	CM6212	QFN-64(7.5x7.5mm)	Tray

3 Features

3.1 USB Compliance

- USB specification 2.0 full-speed/high speed-compatible
- USB audio device class 1.0/2.0-compatible
- USB human interface device (HID) class 1.1-compliant
- Supports USB suspend/resume/reset functions
- Supports control, interrupt, bulk, and isochronous data transfers

3.2 Digital Audio I/O

- 2 stereo I2S serial audio and 1 S/PDIF output interfaces, refer below Table 1 for each audio format support
- 2 stereo I2S serial audio and 1 S/PDIF input interfaces, , refer below Table 1 for each audio format support
- I2S DAC0 support master only
- I2S DAC4 support master/slave
- I2S ADC0 support master/slave
- I2S ADC4 support master/slave

Table 1 (USB Audio Class 1.0)

Interface	Audio Format		Bit Depth
I2S DAC0	I2S(2CH) PCM	192K/176.4K/96K/88.2K/48K/44.1K Hz	16/24/32 bits
	TDM(8CH) PCM	48K/44.1K Hz	16/24 bits
I2S DAC4	I2S(2CH) PCM	192K/176.4K/96K/88.2K/48K/44.1K Hz	16/24 bits
S/PDIF Out	2 CH PCM	192K/176.4K/96K/88.2K/48K/44.1K/32K	16/24 bits
	AC3, DTS Compressed audio data		
I2S ADC0	I2S(2CH) PCM	192K/176.4K/96K/88.2K/48K/44.1K Hz	16/24/32 bits
	TDM(8CH) PCM	48K/44.1K Hz	16/24 bits
I2S ADC4	I2S(2CH) PCM	96K/88.2K/48K/44.1K Hz	16 bits
S/PDIF In	2CH PCM	96K/88.2K/48K/44.1K/32KHz	16 bits
HDA	PCM(2CH Out)	192K/96K/48K/44.1KHz	16/24 bits
	PCM(8CH Out)	96K/48K/44.1KHz	16/24 bits

Table 2 (USB Audio Class 2.0)

Interface	Audio Format		Bit Depth
I2S DAC0	I2S(2CH) PCM	192K/176.4K/96K/88.2K/48K/44.1K Hz	16/24/32 bits
	TDM(8CH) PCM	48K/44.1K Hz	16/24 bits
I2S DAC4	I2S(2CH) PCM	192K/176.4K/96K/88.2K/48K/44.1K Hz	16/24/32 bits
S/PDIF Out	2 CH PCM	192K/176.4K/96K/88.2K/48K/44.1K/32K	16/24 bits
	AC3, DTS Compressed audio data		
I2S ADC0	I2S(2CH) PCM	192K/176.4K/96K/88.2K/48K/44.1K Hz	16/24/32 bits
	TDM(8CH) PCM	48K/44.1K Hz	16/24 bits
I2S ADC4	I2S(2CH) PCM	192K/96K/88.2K/48K/44.1K Hz	16/24/32 bits
S/PDIF In	2CH PCM	192K/96K/88.2K/48K/44.1K/32KHz	16/24 bits
HDA	PCM(2CH Out)	192K/96K/48K/44.1KHz	16/24 bits
	PCM(8CH Out)	192K/96K/48K/44.1KHz	16/24 bits

3.3 Integrated 8051 Micro Processor

- Embedded 8051 micro-processor handles the USB transfers(control, isochronous, interrupt, and bulk)
- Communicate with external peripheral devices(I2C, SPI, GPIO, etc.)
- The MCU speed is programmable from 3.072 ~65.536 MHz
- HID interrupts can be implemented via firmware codes
- Provides maximum HW configuration flexibility with a firmware code upgrade
- VID/PID/product string can be customized via firmware code programming

3.4 Control Interface

- 1 Master I2C control interface to communicate with external devices or EEPROM, the master I2C speed supports standard mode(100KHz) and fast mode(400KHz)
- 1 Slave I2C control interface for external MCU communication, the slave I2C speed supports standard mode(100KHz) and fast mode(400KHz)
- 3 SPI master, supports speed from 32.768M ~ 0.3695Mb/s
- 1 UART
- 18 GPIOs(programmable multi functions I/O), 6 XDs(can be GPIO or other functions)
- 6 PWM LED drivers output

3.5 General

- Embedded USB 2.0 transceiver and power-on reset circuit.
- Bus-power and self-power options
- Single 12MHz crystal input is required (embedded PLL function)
- 12 MHz clock output for external devices.
- Single 5V power supply with embedded 5V to 3.3V regulator.
- Auto detection for high-speed/full-speed
- 3.3V digital I/O pads with 5V tolerance
- Compliant with USB IF certification requirements.
- QFN-64 package (7.5 x 7.5 mm)

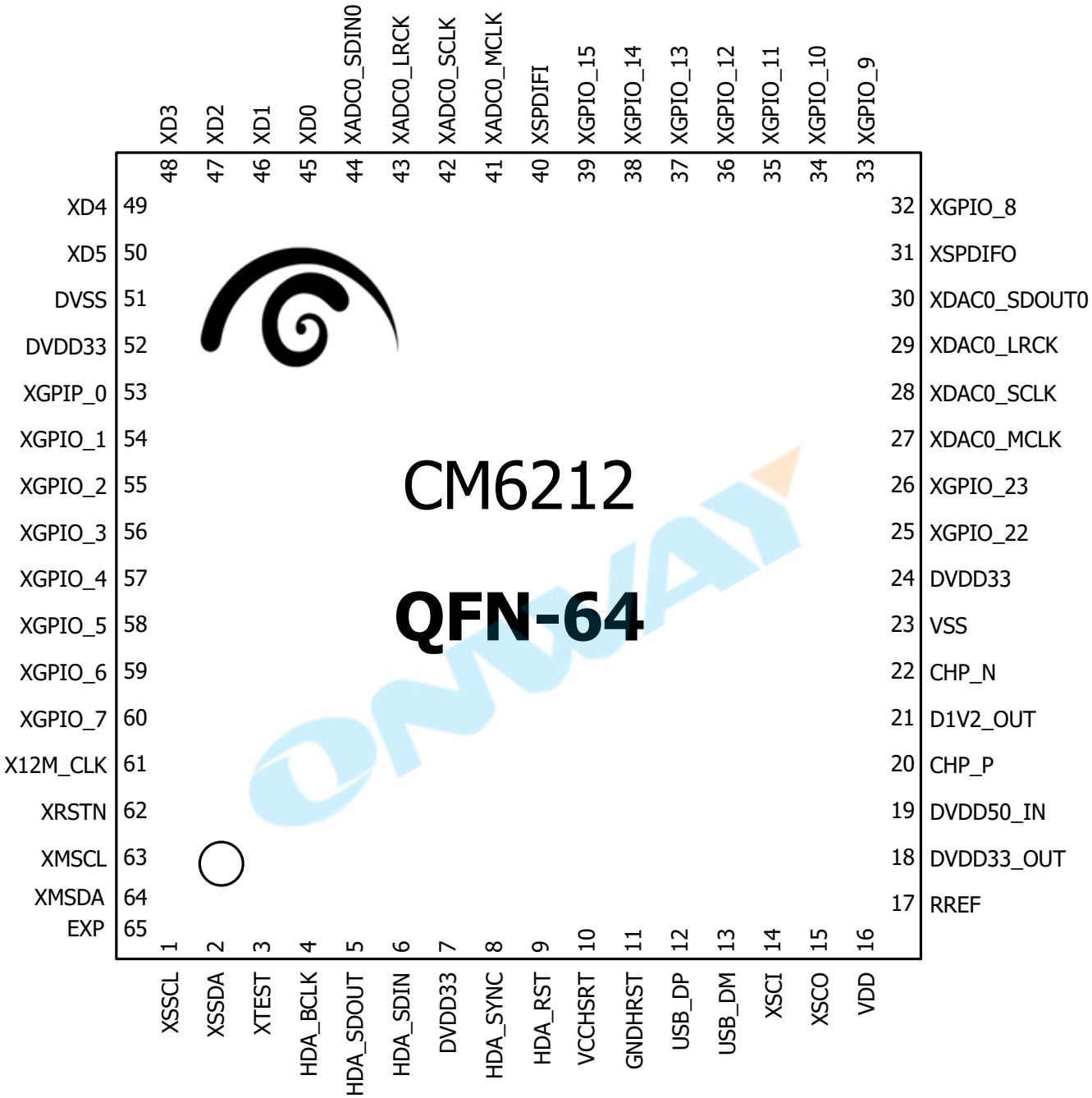
4 Applications

- Game console +PC combo gaming headset: supports 5.1/7.1 surround sounds on multi-platforms (wired or wireless headsets)
- Multi-channels docking/audio box/home theater
- Gaming Headset: USB 5.1/7.1 virtual surround gaming headset with embedded DSP processing (no driver installation required)7.1 virtual surround gaming headset

Applications	Features
7.1 Virtual Gaming Headset	-Two end points -UAC 1.0HS -TDM interface for 8CH 48K/16bit
Audio Box / Motherboard Demand	-CM9881 for 8CH 192K/24bit -UAC 2.0HS -Cmedia Xear function driver
7.1 Real Gaming Headset / Docking	-CM9881 for 8CH 96K/24bit -UAC 1.0HS
Mid-end USB DAC	-External DAC for Stereo 192K/24bit -UAC 1.0HS

5 Pin Assignment

5.1 Pin-out Diagram



5.2 Pin Description

Pin #	Symbol	I/O	Description
Clock			
61	X12M_CLK	-	12MHz clock output
14	XSCI	-	Crystal oscillator input
15	XSCO	-	Crystal oscillator output
USB 2.0 BUS Interface			
17	RREF	-	USB PHY reference resistor. Connect external reference resistor (330Ω±1%)
12	USB_DP	-	USB 2.0 data positive
13	USB_DM	-	USB 2.0 data negative
Power/Ground			
7	DVDD33	PWR	Digital supply voltage 3.3V
19	DVDD50_IN	PWR	Digital supply voltage 5V for digital circuit linear regulator
20	CHP_P	-	Charge-pump positive output, connected to a 2.2uF capacitor
21	D1V2_OUT	PWR	DC-DC 1.25V output (Default)
22	CHP_N	-	Charge-pump negative output, connected to a 2.2uF capacitor
23	VSS	GND	Digital ground supply
24	DVDD33	PWR	Digital supply voltage 3.3V
23	VSS	GND	Digital ground supply
52	DVDD33	PWR	Digital supply voltage 3.3V
18	DVDD33_OUT	PWR	Digital supply voltage 3.3V
10	VCCHSRT	PWR	Digital supply voltage 3.3V
11	GNDHSRT	GND	Digital ground supply
16	VDD	PWR	Digital supply voltage 1.25V, connected to the capacitor filter for digital core
65	EXP	GND	Ground paddle
2 Channel I2S / 8 Channel TDM DAC0 Interface			
27	XDAC0_MCLK	DO	1). I2S DAC0 master clock output 2). DSD bit clock output
28	XDAC0_SCLK	DIO	1). I2S DAC0 bit clock input/output 2). DSD bit clock output 3). TDM DAC SCLK Output
29	XDAC0_LRCK	DIO	1). I2S DAC0 left/right clock input/output 2). DSD channel 1 (or 0, if enable channel switching) data output 3). TDM DAC SYNC Output
30	XDAC0_SDOUT0	DO	1). I2S DAC0 serial data output for channel 0, 1 2). DSD channel 0 (or 1, if enable channel switching) data output 3). TDM DAC DATA Output
2-channel I2S / 8 Channel TDM ADC0 Interface			
41	XADC0_MCLK	DO	I2S ADC0 master clock output
42	XADC0_SCLK	DIO	1). I2S ADC0 bit clock input/output 2). TDM ADC SCLK Output
43	XADC0_LRCK	DIO	1). I2S ADC0 left/right clock input/output 2). TDM ADC SYNC Output

44	XADC0_SDIN0	DI	1). I2S ADC0 serial data input for channel 0, 1 2). TDM ADC DATA Input
HDA Link Interface			
4	HDA_BCLK	DIO	HDA link bit clock (24MHz)
5	HDA_SDOUT	DIO	HDA link serial data out
6	HDA_SDIN	DIO	HDA link serial data in
8	HDA_SYNC	DIO	HDA link frame synchronization
9	HDA_RST	DIO	HDA link reset signal, active low
S/PDIF I/O			
31	XSPDIFO	DO	S/PDIF transmitter
40	XSPDIFI	DI	S/PDIF receiver
GPIO			
25	XGPIO_22	DIO	General purpose input/output 22 (default input)
26	XGPIO_23	DIO	General purpose input/output 23 (default input)
32	XGPIO_8	DIO	1). General purpose input/output 8 (default output) 2). I2S ADC4 master clock output
33	XGPIO_9	DIO	1). General purpose input/output 9 (default output) 2). I2S ADC4 bit clock input/output
34	XGPIO_10	DIO	1). General purpose input/output 10 (default input) 2). I2S ADC4 left/right clock input/output 3). R8051 serial 1 interface transmit data, TXD1
35	XGPIO_11	DIO	1). General purpose input/output 11 (default input) 2). SPI Master chip enable 6 output 3). R8051 serial 1 interface receive data, RXD1 4). I2S ADC4 serial data input for channel 0, 1
36	GPIO_12	DIO	1). General purpose input/output 12 (default input) 2). LED module 4 Output
37	GPIO_13	DIO	1). General purpose input/output 13 (default input) 2). LED module 5 Output
38	GPIO_14	DIO	1). General purpose input/output 14 (default input) 2). LED module 6 Output
39	GPIO_15	DIO	General purpose input/output 15 (default input)
45	XD0	DO	SPI Master clock output
46	XD1	DO	SPI Master data output
47	XD2	DI	SPI Master data input
48	XD3	DO	SPI Master chip enable 0 output
49	XD4	DIO	1). R8051 serial 0 interface receive data, RXD0 2). SPI Master chip enable 2 output

50	XD5	DIO	1). R8051 serial 0 interface transmit data, TXD0 2). SPI Master chip enable 3 output
53	XGPIO_0	DIO	1). General purpose input/output 0 (default input) 2). I2S DAC4 master clock output
54	XGPIO_1	DIO	1). General purpose input/output 1 (default input) 2). I2S DAC4 bit clock input/output
55	XGPIO_2	DIO	1). General purpose input/output 2 (default input) 2). I2S DAC4 left/right clock input/output
56	XGPIO_3	DIO	1). General purpose input/output 3 (default input) 2). I2S DAC4 serial data output for channel 0, 1
57	XGPIO_4	DIO	1). General purpose input/output 4 (default input) 2). LED module 1 Output
58	XGPIO_5	DIO	1). General purpose input/output 5 (default input) 2). LED module 2 Output
59	XGPIO_6	DIO	1). General purpose input/output 6 (default input) 2). LED module 3 Output
60	XGPIO_7	DIO	General purpose input/output 7 (default input)
Control Interface			
63	XMSCL	DIO	I2C Master serial clock
64	XMSDA	DIO	I2C Master serial data
1	XSSCL	DIO	I2C Slave serial clock
2	XSSDA	DIO	I2C Slave serial data
Miscellaneous			
62	XRSTN	DI	Reset input, active low
3	XTEST	DI	Test mode input (Connect to ground)

AI: Analog Input

AO: Analog Output

AIO: Analog Input/Output

DI: Digital Input

DO: Digital Output

DIO: Digital Input/Output

6 Function Description

6.1 USB Topology

The CM6212 USB Topology is programmable by changing firmware. If the internal firmware is empty, the CM6212 will report a HID device to the system. It is use to load the firmware.

6.2 USB Endpoint

All USB devices must support a control pipe at endpoint number zero (default control pipe). The full speed and high speed devices may support up to a maximum of 16 endpoints. The endpoint table of CM6212 is listed as follows.

EndpointNumber	Direction	Type	Description
0	IN	Control	
	OUT		
1	IN	Bulk, Isochronous	Audio, Recording DMA #R5
	Out	Bulk A	
2	IN/OUT	Bulk B	
3	IN	Feedback	Audio, Playback DMA #P5
	OUT	Isochronous	
4	IN/OUT	Interrupt A	
5	IN	Feedback	Audio, Playback DMA #P0
	OUT	Isochronous	
6	IN		
	OUT		
7	IN		
	OUT		
8	IN	Isochronous	Audio, Recording DMA #R0
9	IN		
A	IN		
B	IN		
	OUT		
C			
D	IN		
E	IN	Isochronous	Audio, Recording DMA #R4
F	IN/OUT	Interrupt B	

6.3 I2S Interface

The main audio interface of the CM6212 is I^2S, which has three clock signals, MCLK, BCLK and LRCK, and at least one data line depending on the channels supported. One data line contains two channels. The three I^2S clock symbols are explained below.

MCLK = main clock.
BCLK = bit clock.
LRCK = left and right clock.

6.3.1 The Basics of I2S Bus

Both master and slave modes of I2S are supported by the I2S interfaces of the CM6212, namely I2S DAC0, I2S ADC0. Master mode means BCLK and LRCK are provided by the CM6212 as shown in Fig. 7.3.1(a). On the contrary, slave mode means BCLK and LRCK are provided by the I2S codecs as depicted in Fig. 7.3.1(b).

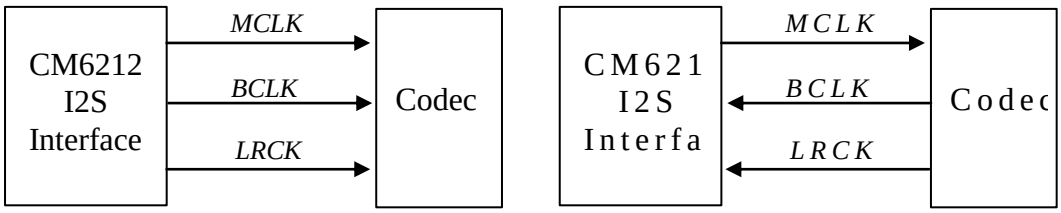


Fig. 7.3.1 (a) Master mode

Fig. 7.3.1 (b) Slave mode.

Fig. 7.3.2 indicates the basic waveform of I2S. Note that BCLK is generated at the positive edges of MCLK with the ratios 1, 1/2, 1/4, or 1/8, and LRCK is generated at the negative edges of BCLK with the ratios 1/64, 1/128, 1/256. Data bits are transited at the negative edges of BCLK, and are sampled at the positive edges of BCLK. In case of playback, CM6212 is the data transmitter and the codec is the data receiver. As for recording, the roles of CM6212 and codec are reversed.

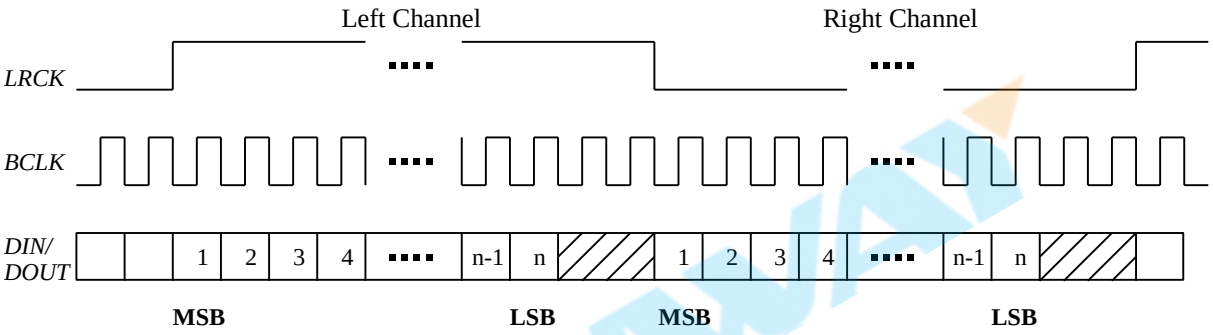


Fig. 7.3.2 The basic timing diagram of the I2S interface.

For the I2S DAC controller, the audio data is transformed from the parallel format to the serial format before transmitted. Then, the bit data is shifted out one by one with the MSB first via DOUT signal. If the I2S DAC controller is set to 32 bits, at least 32 BCLK clocks must exist in both LRCK left and right channels. In the same manner, the audio data is transformed from the coming serial format to the parallel format for a I2S ADC controller.

6.3.2 Left Justified Mode

In the left justified mode of the I2S DAC controller, the MSB data bit is clocked out by the CM6212 at the negative edge of BCLK which is aligned to the transition of LRCK. In the left justified mode of I2S ADC controllers, the MSB data bit is clocked out by codecs and sampled by the CM6212 at the first positive edge of BCLK which follows a LRCK transition. LRCK is high during left channel transmission and low during right channel transmission in the left justified mode. Fig. 7.3.2 shows all of these.

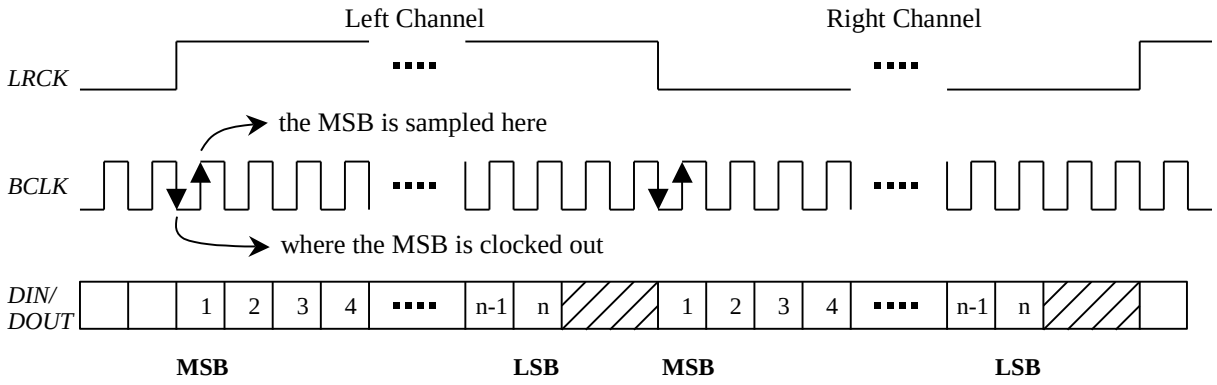


Fig. 7.3.2 Left justified mode timing diagram of I2S interface.

6.3.3 I2S Mode

In the I2S mode of the I2S DAC controller, the MSB data bit is clocked out by CM6212 at the first negative edge of BCLK which follows a LRCK transition. In the I2S mode of I2S ADC controllers, the MSB data bit is clocked out by codecs and sampled by the CMA6635 at the second positive edge of BCLK which follows a LRCK transition. LRCK is low during left channel transmission and high during right channel transmission in the I2S mode. Fig. 7.3.3 indicates all of these.

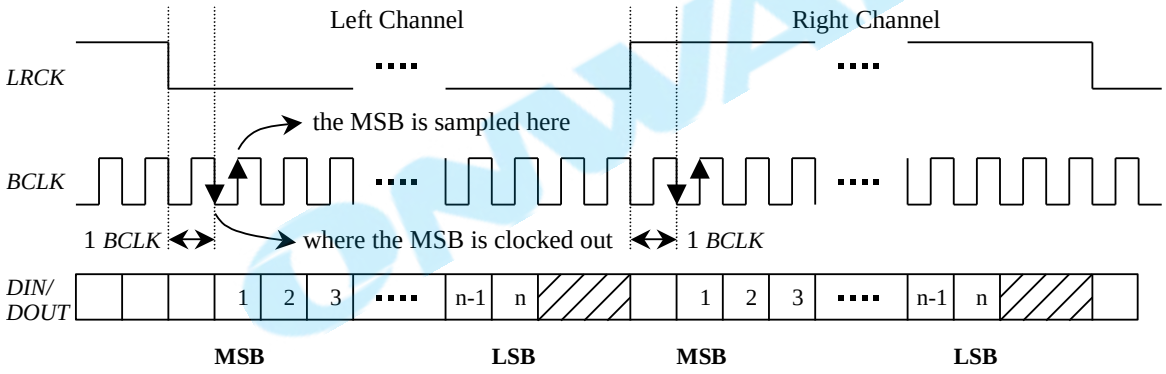


Fig. 7.3.3 I2S mode timing diagram of I2S interface.

6.4 S/PDIF Interface

SPDIF is an audio transmission format in digital domain. The data stream format is illustrated in Fig. 7.4.1. The maximum unit of the S/PDIF stream is a block. A block is composed of 192 frames, and each frame is composed of two subframes. One frame contains one audio sample, so the frame rate is equal to the sampling rate. The left channel audio data is carried by bit slot 4-27 (or time slot 4-27) of subframe A, and right channel is carried by bit slot 4-27 of subframe B. The Sync slot takes preamble signal which is used to label the beginning of a subframe. There are three types for preamble signal, the first is B type, used only in the first subframe of a block; the W type, used in all subframe B; the M format, used in all subframe A, besides the first subframe of a block. The block format is shown in Fig. 7.4.1. The logical level at the start of a bit is always inverted to the level at the end of the previous bit. The level at the end of a bit is equal (a 0 transmitted) or inverted (a 1 transmitted) to the start of that bit.

The S/PDIF data signal is coded by the “biphase-mark-code,” which is a kind of phase modulation. It is illustrated in Fig. 7.4.2. The base clock of a S/PDIF signal is twice the bit rate, and the frequency of the base clock is only

determined by the sampling rate. The period of the base clock is called the Unit interval (UI). For example, for a 48KHz 2-channel S/PDIF signal, the frame rate is also 48KHz, so a frame period is 20.833us, and a subframe period is 10.416us. A subframe contains 32-bit slot, so a bit slot period is 325.52ns. As we said above, the base clock is twice the bit rate. Therefore, the period of the base clock is 162.76ns. In other words, the frequency of base clock is 6.144 MHz. Bi-phase coding can prevent PCM data from DC isolated and insensitive to level polarity. A maximum up to 24 data bits can be transmitted by the S/PDIF signal, and the sequence is from LSB to MSB.

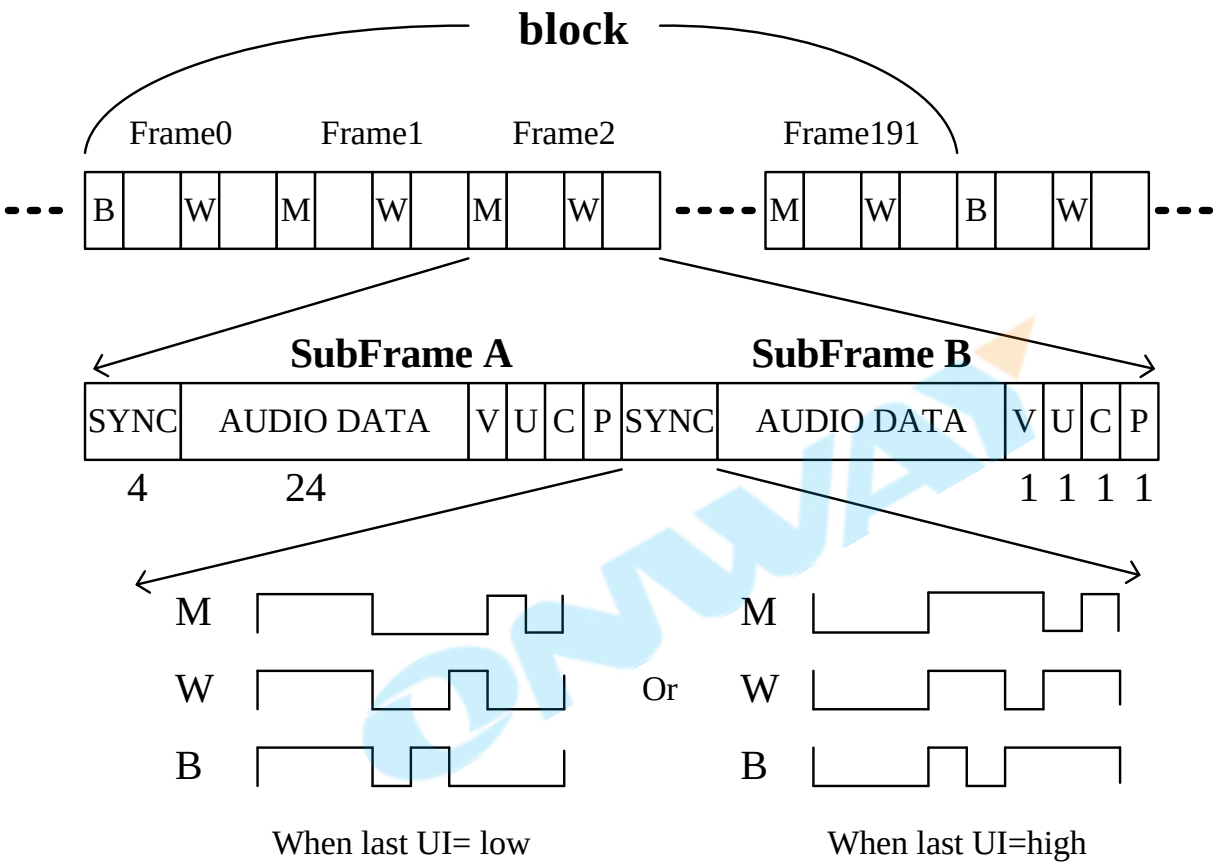


Fig. 7.4.1 S/PDIF Frame format.

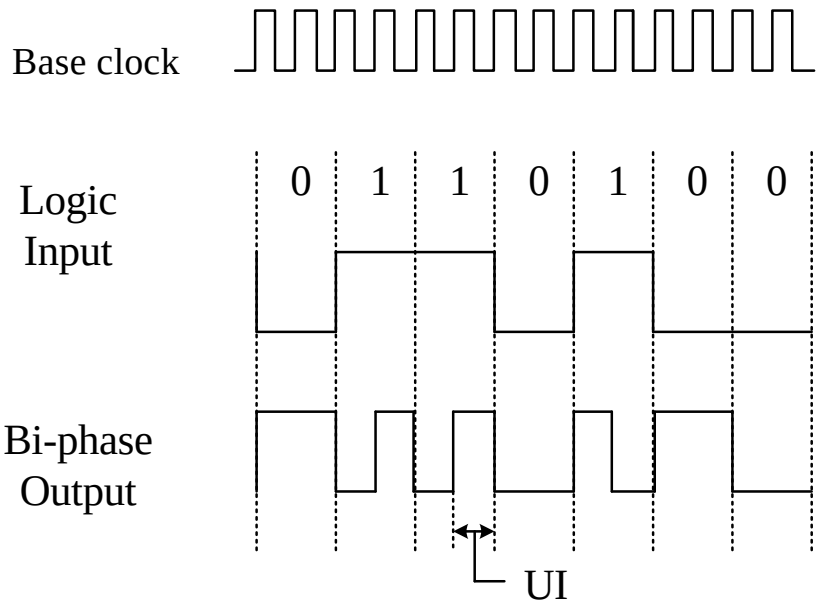


Fig. 7.4.2 S/PDIF biphase-mark-code (BMC).

6.5 I2C, Two-Wire Interface

The 2-wire master and slave serial buses are designed separately in the CM6212. There are two reasons which let us make such a decision. The first reason is that the separated 2-wire master and slave buses are easier to design, and the second reason is that the 2-wire master bus pins have been shared with SPI interface. In the most applications, the SPI interface is the one that is chosen to control the codecs, so the 2-wire slave bus cannot combine with the 2-wire master bus.

6.5.1 The Concept of I2C, Two Wire Interface

The 2-wire bus, as its name reveals, has 2 lines. One is the serial clock line (*SCL*), and the other is the serial data line (*SDA*). Both of them are operated under open drain. That means if the 2 lines are not driven by a master or a slave, they are pulled high by the external pull-up resistors as indicated by Fig. 7.5.1. A device connected on the bus can be recognized as a master or a slave when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave. Another concept that we should know is the transmitter-receiver relation. *The transmitter is the device which sends data to the bus, and receiver is the device which receives data from the bus.* Note that the definition of transmitter-receiver is different from that of master-slave. We will use these terms to explain 2-wire read/write transactions later. The CM6212 use 7 bits to address the slave devices such as codecs, so theoretically, the 2-wire bus is able to connect 128 slave devices. However, in the audio system application, the limitation is on the codecs, not on the CM6212. Usually, the codecs which support 2-wire bus only have one or two pins to select their address. Therefore, two or four codecs is allowed in the system indicated by Fig. 7.5.1, unless the codecs are from different manufactures. In the MCU application, the CM6212 is a slave device, and it can be addressed by the MCU via four different addresses, 0001000b, 0001001b, 0001010b, 0001011b.

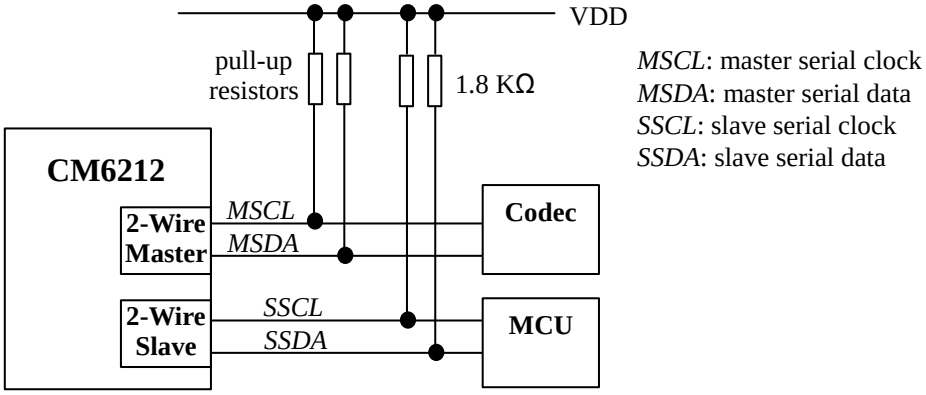


Fig. 7.5.1 The connection of 2-wire master and slave buses.

6.5.2 Start and Stop Condition

For a 2-wire bus transaction, the start and stop condition is defined as follows and shown in Fig.7.5.2.

- Start: a high to low transition on the *SDA* line while *SCL* is high.
- Stop: a low to high transition on the *SDA* line while *SCL* is high.

Start and stop conditions always generated by the master device. The bus is considered to be busy after the start condition. The bus is considered to be free again after the stop condition.

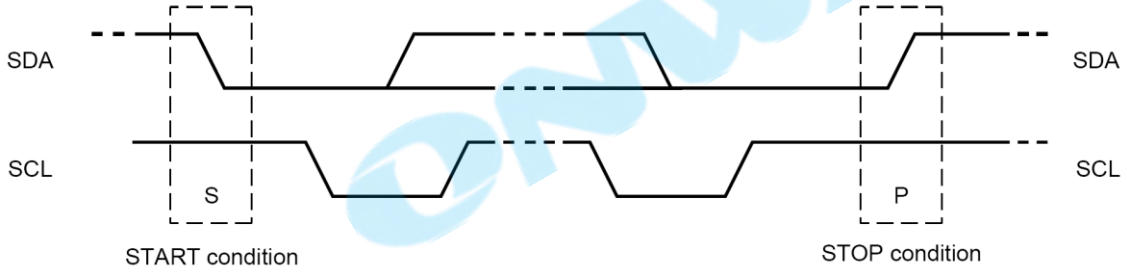


Fig. 7.5.2 Start and stop conditions of 2-wire bus.

6.5.3 Bit Transfer

The data on the *SDA* line must be stable during the high period of the clock. The state of the data line can only transit when the clock signal on *SCL* line is low. The bit transfer is indicated in Fig. 7.5.3.

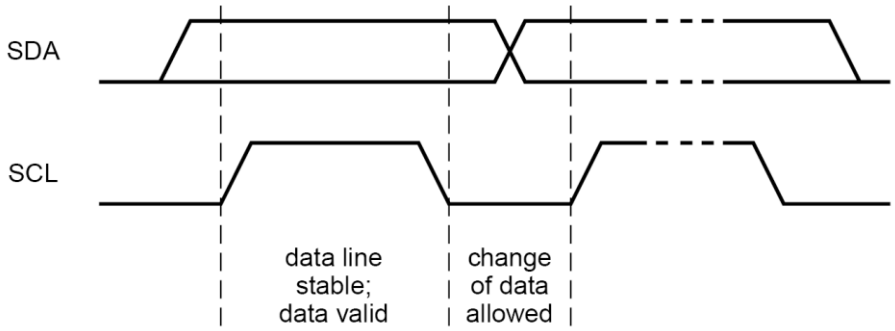


Fig. 7.5.3 Bit transfer of 2-wire bus.

6.5.4 Transferring Data with Read/Write Transactions and Acknowledge

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is 3 or 4 bytes in the CM6212. The first byte is always the address byte which is composed of the 7-bit address and 1 read/write bit, listed in Fig. 7.5.4.1 For a write transaction, the second byte is called *Memory Address Pointer* (MAP), which is usually used to indicate the target register in the slave device that the followed third and fourth bytes will be applied on. For a read transaction (only 3 bytes), the second and third bytes is the data returned by the slave device. Each byte has to be ended by an acknowledge bit. Data is transferred with the most significant bit first.

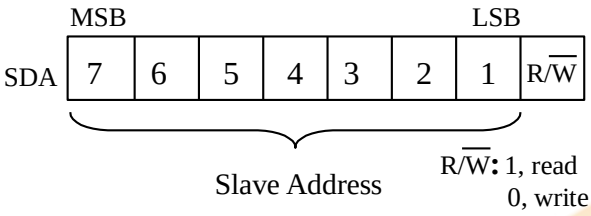


Fig. 7.5.4.1 The first byte after start condition.

The 2-wire master bus of the CM6212 supports read/write transactions. All these transactions are depicted in Fig. 7.5.4.2 to give a whole picture about what the CM6212 can do.

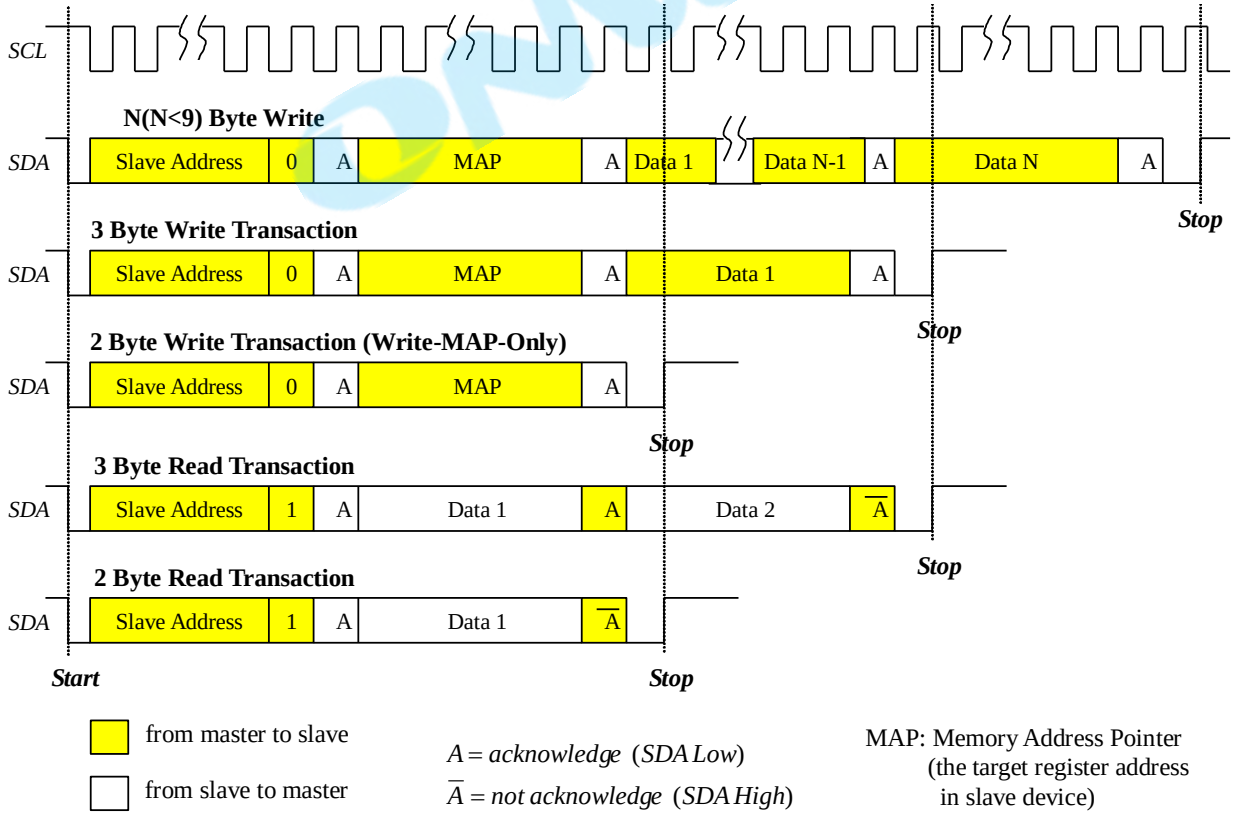


Fig. 7.5.4.2 The 5 basic transactions of the 2-wire master bus supported by the CM6212.

In a read transaction, usually the slave device returns the data of the register whose address is in the MAP. If the read transaction is a 3 byte read transaction, the second returned byte is the data in the (address+1) register. Therefore, the action of obtaining the data in slave device is composed of two transactions, namely a 2 byte write transaction (Write-MAP-Only) followed by a read transaction. For the convenience of users, we have designed an auto read transaction, shown in Fig. 7.5.4.3, which is actually the combination of a write and a read transactions.

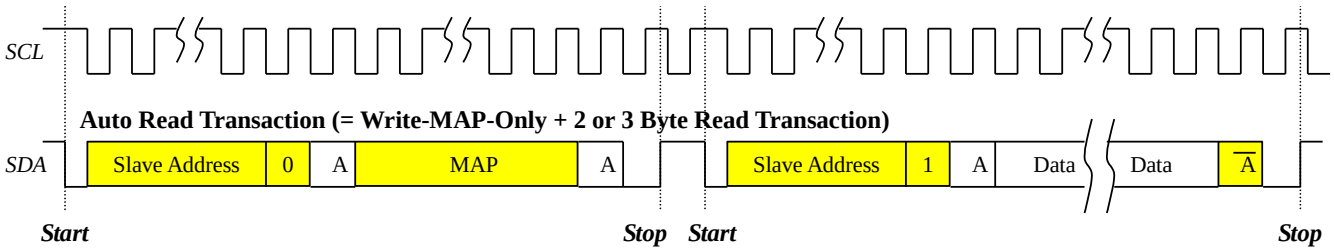


Fig. 7.5.4.3 Auto read transaction in the CM6212.

Data transfer with acknowledge is obligatory. The transmitter release SDA line during the acknowledge clock pulse. Then, the receiver must pull down the SDA line during the acknowledge clock pulse so that it remains low for the entire acknowledge clock high period. This is shown in Fig. 7.5.4.4. When a salve does not acknowledge the slave address byte. For example, it is unable to receive or transmit because it is performing some real-time function. The data line should be left high by the slave. The master can then generate either a stop condition to abort the transfer, or a repeated start condition to start a new transfer.

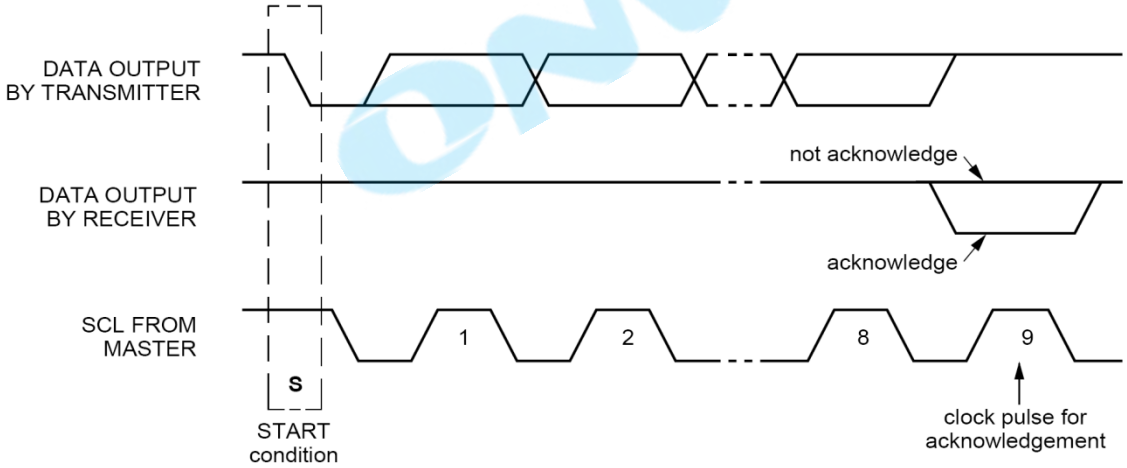


Fig. 7.5.4.4 Acknowledge of the 2-wire bus.

For a read transaction, after the slave address byte is transmitted and acknowledged by slave device, the role of master-transmitter is altered to become master-receiver, and the original slave-receiver is altered to become slave-transmitter. This conception can be easily observed in Fig. 7.5.4.3 and 7.5.4.4, where we use yellow and white blocks to denote the data bit transfer direction. Yellow means the data direction is from the master to the slave. White means the data direction is from the slave to the master. Meanwhile, in a read transaction, the master-receiver must signal the end of the data to the slave transmitter by generating a not-acknowledge ($\overline{A}$) on the last byte that was clocked out of the slave-transmitter. The slave-transmitter should release the *SDA* line to allow the

master to generate a stop or repeated start condition.

6.5.5 Synchronization

The synchronization of the 2-wire bus in the CM6212 can be described in two aspects. The first aspect is the synchronization used in arbitration. Although we did not implement arbitration, we did implement clock synchronization. Clock synchronization is used when there are more than two masters connected on the bus. A high to low transition on the *SCL* line will cause the concerned masters start counting the clock low period. Before the clock high state is reached, the masters will hold the *SCL* line in low state. However, the low to high clock transition of one of the masters may not change the state of the *SCL* line if another master's clock is still in low period (because the *SCL* line of the devices are wire-AND connected by open-drain technique). Therefore, the *SCL* line will be held low by the device with the longest clock low period. The other devices with shorter low period, including the CM6212, enter a high wait state during this time. Figure 7.5.5.1 listed below is the timing of clock synchronization.

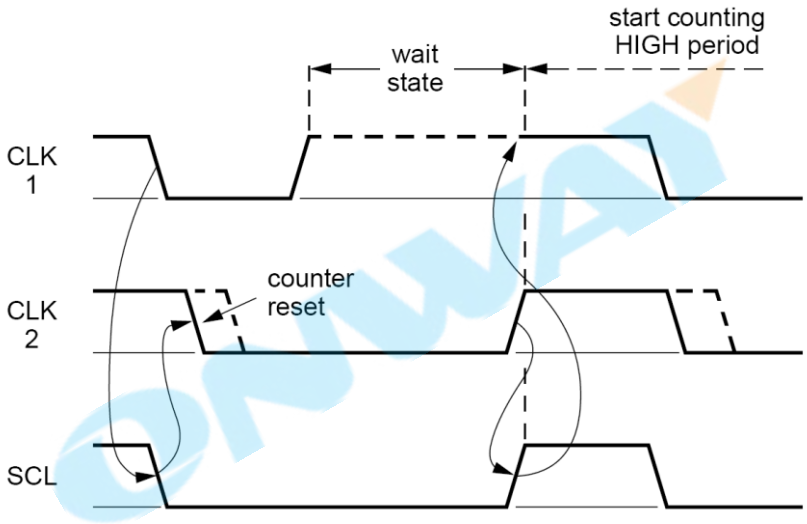


Fig. 7.5.5.1 Clock synchronization for more than two masters in the bus.

Another aspect of synchronization is the data synchronization between master and slave. If a slave cannot receive or transmit another complete byte of the data until it has performed some other function, for example servicing an internal interrupt or waiting for the driver to prepare the data needed, the salve can hold the clock line *SCL* low to force the master into a wait state. Data transfer then continues when the slave is ready and releases the clock line *SCL*. The data synchronization is shown in Fig. 7.5.5.2.

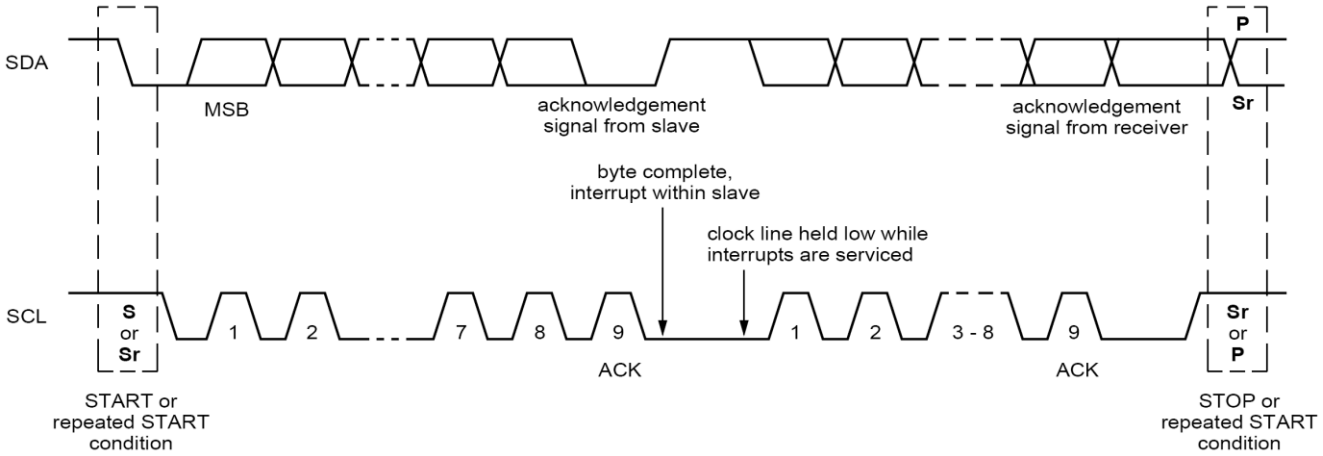


Fig. 7.5.5.2 The data synchronization of the 2-wire master and slave buses in the CM6212.

6.5.6 Standard Mode and Fast Mode

Both the 2-wire master and slave buses in the CM6212 can support standard mode transfer and fast mode transfer. The data transfer rate of the standard mode is up to 100 Kbits/sec, and the fast mode is up to 400 Kbits/sec. The clock timing of these modes are listed in Fig. 7.5.6 and Table 7.5.6

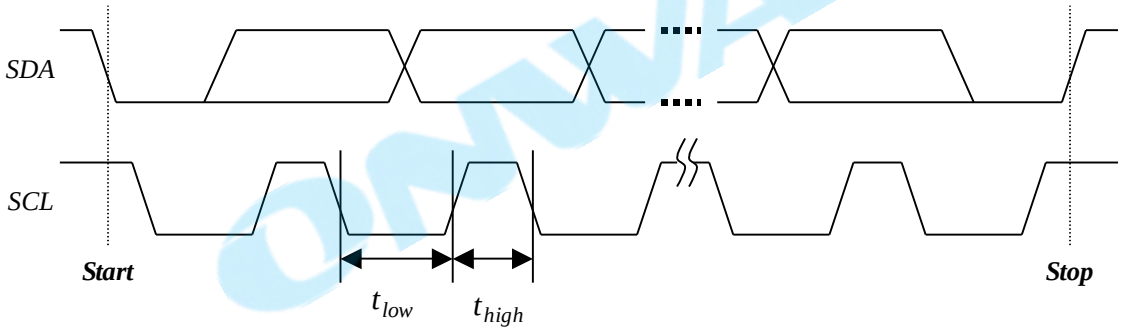


Fig. 7.5.6.1 Standard mode and fast mode timing.

Table 7.5.6 Standard mode and fast mode timing.

Parameter	Symbol	Standard mode		Fast mode		Unit
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	KHz
Low period of *SCL* clock	t_{low}	4.8	—	1.3	—	μS
High period of *SCL* clock	t_{high}	4.8	—	0.6	—	μS

6.6 TDM(Time-Division Multiplexing)

There are two TDM interfaces in CM6212. One is TDM-out and another is TDM-in. TDM has two clock signals and one data signal used to transmit 8-channel data. Supported audio data format are Mode 1 and Mode 2.

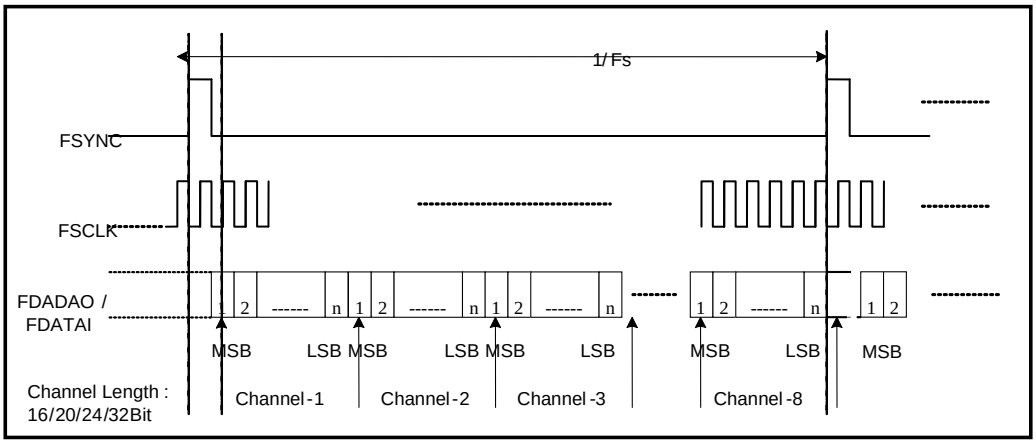


Fig. 7.6.1 TDM Mode 1

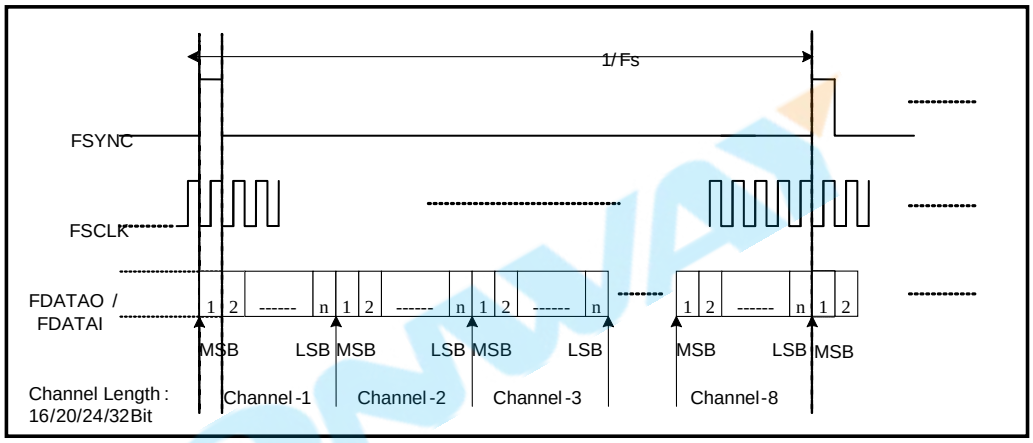


Fig. 7.6.2 TDM Mode 2

6.7 SPI Interface

The SPI128 module is a typical type of SPI interface for external SPI devices. It could most support 128 bytes in a SPI transfer. It supports 4 kinds of modes, which is two kinds of clock polarity and two kinds of phase polarity. Besides the typical SPI function for external SPI devices, the SPI128 module has the FIFO control function for wireless applications. It could directly move in or out the SPI data to recording or playback SRAM through the SPI128 module internal 128 bytes SRAM.

6.7.1 The SPI128 interface Typical Transfer

The typical SPI128 Interface has 4 communication signals, which are SPI_DIN, SPI_DOUT, SPI_CLK and SPI_CEN. The SPI128 supports up to 8 external devices, user could use the chip select register to decide which one is selected. The SPI128 could configure the clock and phase polarity. Figure 7.6.1.1 and 7.6.1.2 describe the operation behaviors. When the clock polarity is set to zero (sckpol=0), means the SPI clock level is low when SPI is idle. When the clock polarity is set to one (sckpol=1), means the SPI clock level is high when SPI is idle.

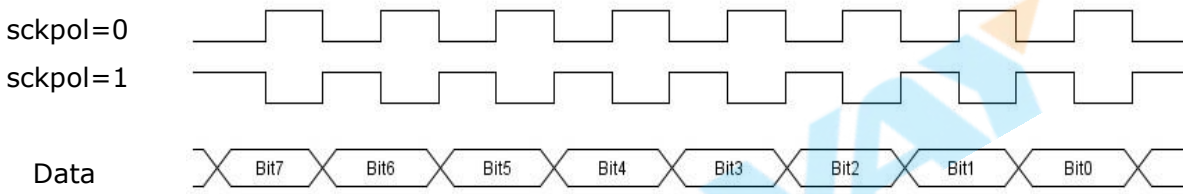


Fig 7.6.1.1, phase polarity = 0

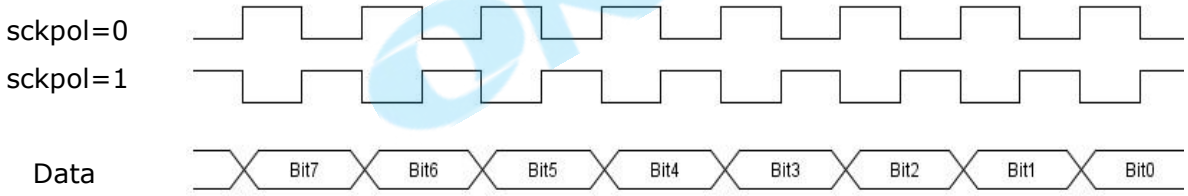


Fig 7.6.1.2, phase polarity =

- At sckpol=0: SPI clock level is low when SPI is idle
  - for phase polarity = 0, data are captured on the rising edge of SPI_CLK and data is propagated on the falling edge of SPI_CLK.
  - for phase polarity = 1, data are captured on the falling edge of SPI_CLK and data is propagated on the rising edge of SPI_CLK.
- At sckpol=1: SPI clock level is high when SPI is idle
  - for phase polarity = 0, data are captured on the falling edge of SPI_CLK and data is propagated on the rising edge of SPI_CLK.

For phase polarity = 1, data are captured on the rising edge of SPI_CLK and data is propagated on the falling edge of SPI_CLK.

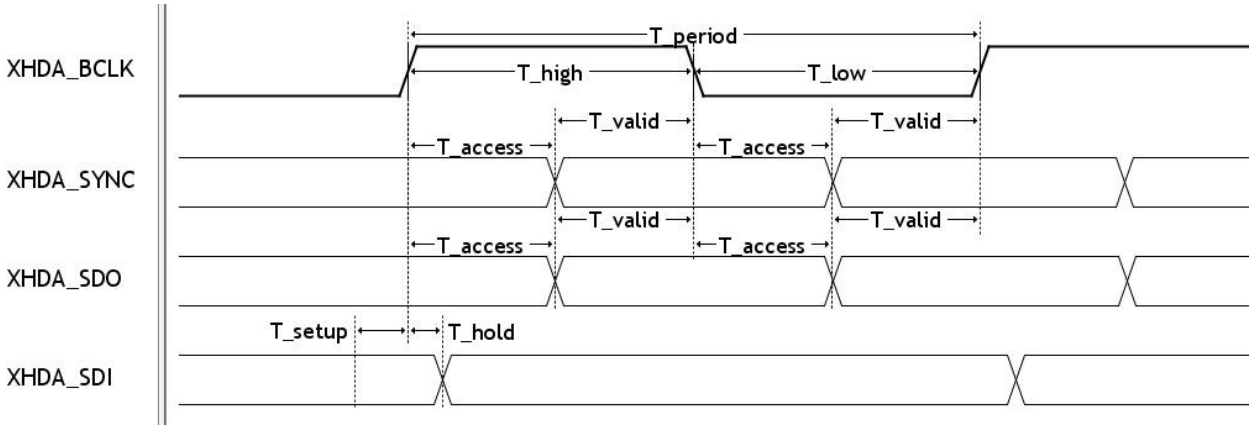
6.8 GPIO

All the GPIO pins can be configured as input or output by the GPIO direction control registers and also can be configure as remote wake up input pin. If they are assigned as outputs, then the contents in the GPIO data registers will be reflected to the corresponding GPIO pins. If they are assigned as inputs, they can be used for jack activity detection. If a speaker is plugged or unplugged, the state of the pin connected with that jack will be changed. As a result, an interrupt is issued to R8051, and an interrupt mask control bit is utilized to decide if the interrupt from that corresponding GPIO pin should be sent. After receiving the interrupt, R8051 must read the GPIO data register (address offset 0x0300h) to discover what pins have changed their states. Then, the R8051 will make some appropriate manipulation in response to the jack activity.

CM6212 supports two kinds of Remote-wakeup. One is hardware Remote-wakeup, and the other is software Remote-wakeup. When in Configuration, CM6212 has to report the host via the descriptor whether CM6212 supports the Remote-wakeup or not. If CM6212 reports it supports Remote-wakeup and the host also supports Remote-wakeup, the host will issue the request of Set-feature to enable the Remote-Wakeup feature. If the user selects hardware Remote-wakeup, the user has to select one of the GPIOs to configure as a remote wakeup pin. If there is a transition from 0 to 1 on this pin, that will cause a remote-wakeup to wake up the host from the suspend state. The transition can be from outer world or from the control of the R8051. If the transition is from the control of the R8051, this is called Software Remote-wakeup. Software Remote-wakeup is implemented by the register. If the user selects software Remote-wakeup, the 8051 has to write the register to cause the transition from 0 to 1 to wake up the host.

CM6212 has a de-bouncing circuit to filter the interrupt to R8051. There are two options to select which are 16ms and 8ms. The user can select one option to use according to their application.

6.9 HDA Control Interface Timing



Parameter	Symbol	Min.	Typ.	Max.	Units
XHDA_BCLK frequency		23.99	24	24.0024	ns
Total period of XHDA_BCLK	T_period	41.363	41.67	41.971	ns
High phase of XHDA_BCLK	T_high	18.75	-	22.91	ns
Low phase of XHDA_BCLK	T_low	18.75	-	22.91	ns
XHDA_BCLK jitter	-	-	150	300	ns
Time duration for which XHDA_SDO is valid after the XHDA_BCLK edge	T_access	11	-	11	ns
Data Valid Time	T_valid	7.75	-	11.91	ns
Setup for XHDA_SDI at rising edge of the XHDA_BCLK	T_setup	7	-	-	ns
Hold for XHDA_SDI at rising edge of the XHDA_BCLK	T_hold	2	-	-	ns

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ	Max.	Unit
Storge temperature	T_S	-40	-	125	°C
supply voltage	DVDD50_IN	-	-	5.5	V
ESD (Body mode)	HBM	-	±4000	-	V
ESD (Machine mode)	MM	-	±200	-	V

7.2 Recommended Operation Conditions

Parameter	Symbol	Min.	Typ	Max.	Unit
Operating ambient temperature	T_A	0	25	70	°C
supply voltage	DVDD50_IN	4.5	5	5.5	V
Crystal Clock	-		12.000		MHz

7.3 Static Characteristics

Parameter		Min.	Typ	Max.	Units
Input voltage range	DI	0		5.5	V
Output voltage rage	DO	0		3.3	V
Input Voltage High	VIH	0.7*DVDD33	DVDD33	5.5	V
Input Voltage Low	VIL	-	-	0.3*DVDD33	V
Output Voltage High	VOH	0.9*DVDD33	-	-	V
Output Voltage Low	VOL	-	-	0.1*DVDD33	V

7.4 Power Consumption

Test Conditions: DVDD50_IN, DVSS =0V, TA=+25°C, MCU Clock = 3MHz.
Sample Rate=48kHz, 24Bits, Operation: I2S output and I2S input,
I2S output and I2S input = Gain 0dB

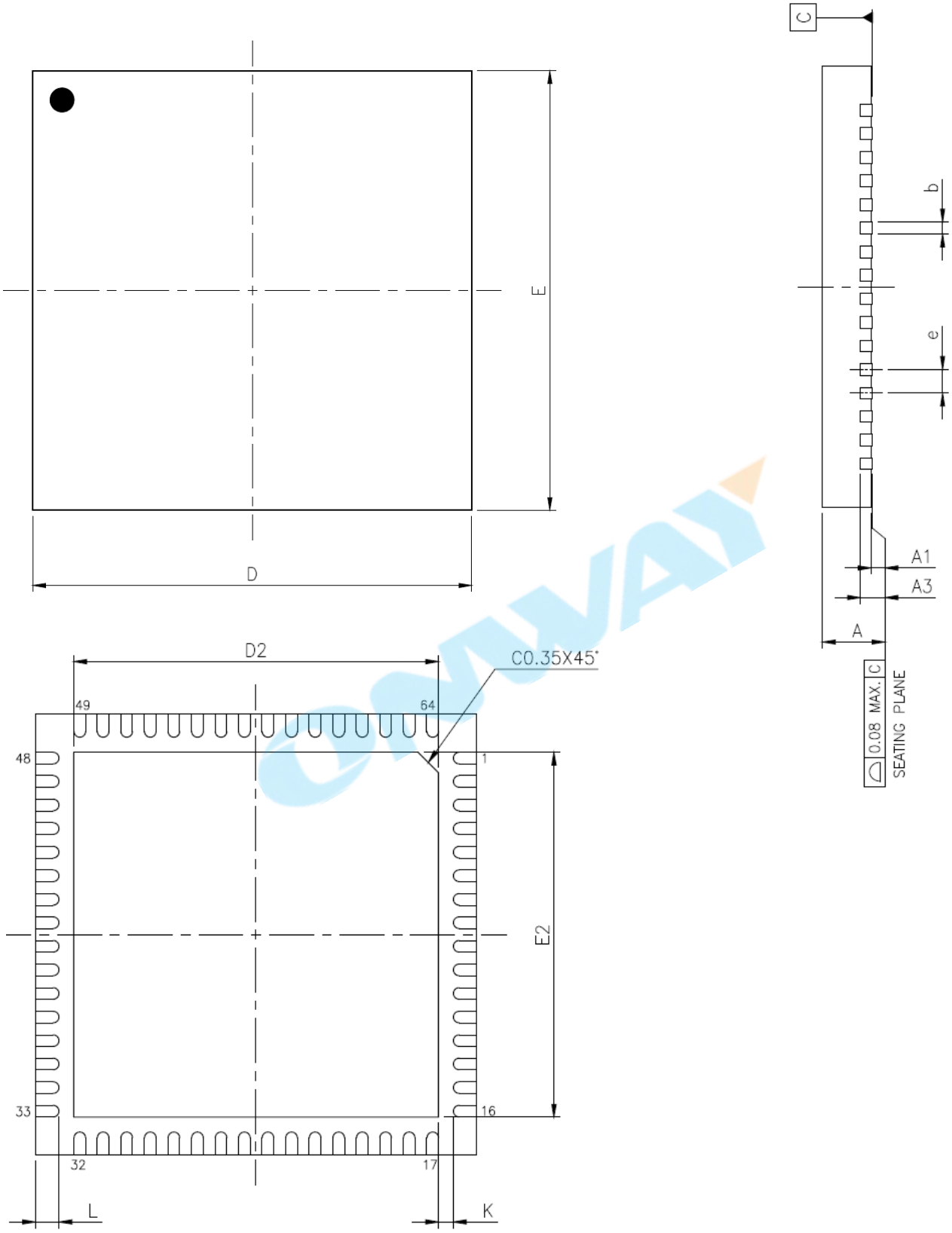
Parameter	Min.	Typ	Max.	Units
Total power consumption (Playback + Record)	-	48	-	mA
Standby power consumption	-	41.6	-	mA
Suspend mode power consumption	-	2.3	-	mA

7.5 DC Characteristics

Test Conditions: DVDD50_IN=5V, DVSS =0V, TA=+25°C

Parameter	Symbol	Min.	Typ	Max.	Units
High-level input voltage	Vih	2.4	-	5.3	V
Low-level input voltage	Vil	-	-	0.8	V
High-level output voltage	Voh	2.4	-	-	V
Low-level output voltage	Vol	-	-	0.4	V
SPDIF High-level input voltage	-	1.75	-	-	V
SPDIF Low-level input voltage	-	-	-	1.55	V

8 Package Dimensions



PKG CODE	VQFN(Y764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
252X25' MIL	6.15	6.20	6.25	6.15	6.20	6.25	V	V	N/A

— End of Datasheet —

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